Data Sheet

B50612D

10/100/1000BASE-T Gigabit Ethernet Transceiver

GENERAL DESCRIPTION

The Broadcom® B50612D is a triple-speed 1000BASE-T/100BASE-TX/10BASE-T Gigabit Ethernet (GbE) transceiver integrated into a single monolithic CMOS chip. The device performs all physical-layer functions for 1000BASE-T, 100BASE-TX, and 10BASE-T Ethernet on standard Category 5 UTP cable. 10BASE-T can also run on standard Category 3, 4, and 5 UTP. The B50612D is a highly integrated solution combining digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders, decoders, echo cancellers, crosstalk cancellers, and all required support circuitry. Based on Broadcom's proven digital signal processor technology, the B50612D is designed to be fully compliant with RGMII, allowing compatibility with industry-standard Ethernet MACs and switch controllers.

Designed for reliable operation over worst-case Category 5 cable, the B50612D automatically negotiates with its link partner to determine the highest possible operating speed. The device detects and corrects most common wiring problems. The B50612D features CableChecker™ diagnostics, which detect common cable problems including shorts, opens, and cable length.

FEATURES

- Single-chip integrated triple-speed Ethernet transceiver
- 1000BASE-T IEEE 802.3ab
- 100BASE-TX IEEE 802.3u
- 10BASE-T IEEE 802.3™
- Supports only RGMII MAC interface
- Supports SOFT-RESET
- IDDQ with Soft Recovery (IDDQ-SR mode)
- IDDQ with Signal Detect (IDDQ-SD mode)
- Ethernet@Wirespeed™
- Integrated voltage regulator
- Trace matched output impedance
- Lineside loopback
- Low EMI emissions
- Cable plant diagnostics
- Robust CESD tolerance
- Support for jumbo packets up to 10 KB
- Detection and correction of pair swaps
- (MDI crossover), pair skew, and pair polarity
- Advanced power management
- IEEE 1149.1 (JTAG) boundary scan
- IEEE 802.3az-compliant support
  - Support for native EEE MACS
  - Support for legacy non-EEE MAC using AutogrEEEn mode
- Super-isolate mode
- 48-pin MLP packages

APPLICATIONS

- GbE switches and uplinks

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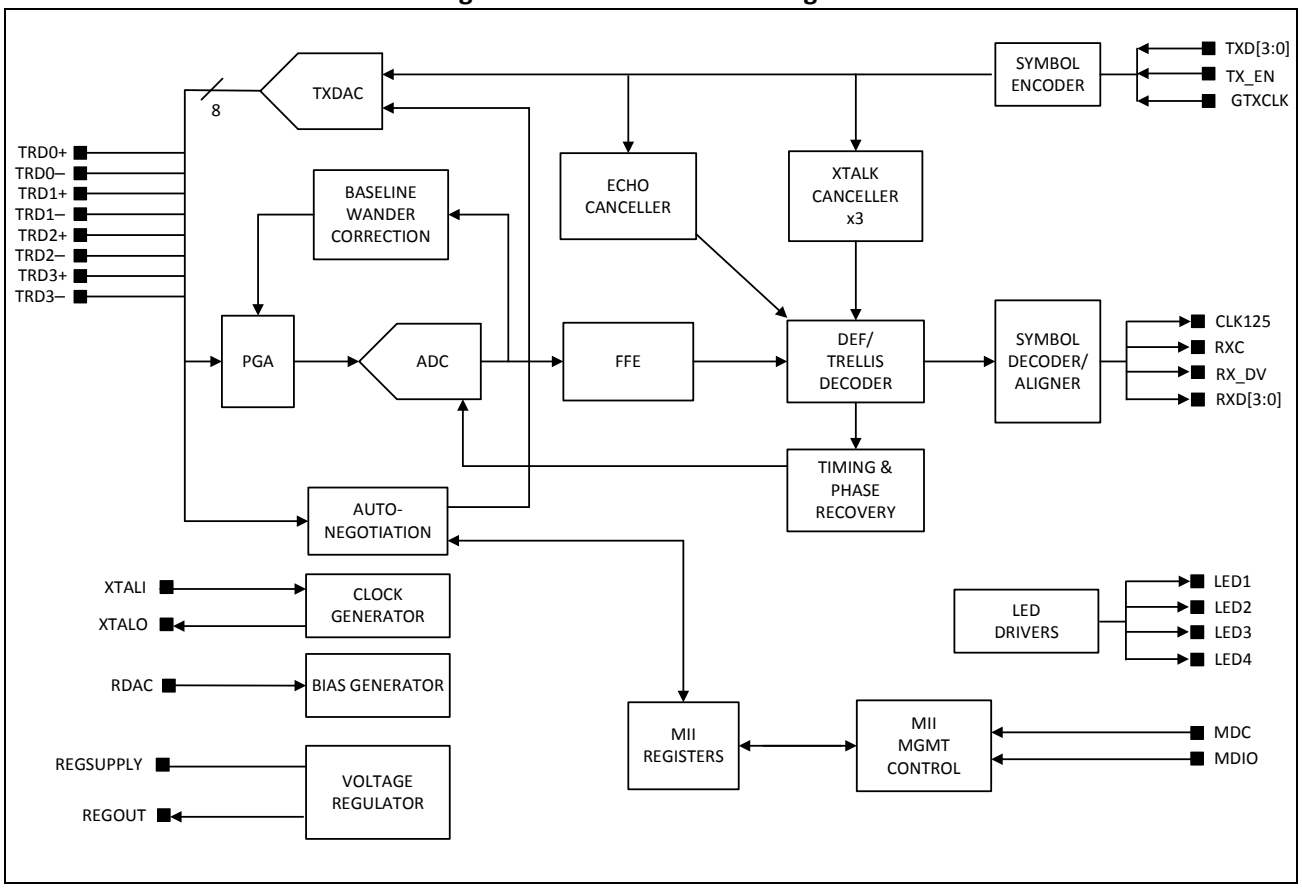
Figure 1: Functional Block Diagram



Revision History

Revision	*Date*	*Change Description*
B50612D-DS100-R	12/18/13	Initial release.

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List of Figures

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

Table of Contents

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

List of Tables

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® B50612D. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

Acronyms and abbreviations in this document are also defined in Appendix A: "Acronyms and Abbreviations," on page 160.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

References

The references in this section may be used in conjunction with this document.

Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	*Number*	*Source*
Broadcom Items		
[1] 10/100/100BASE-T Linking Issues Application Note	AUTONEG-AN10x-R	Broadcom CSP
[2] How to Design with the B50612D	B50612D-AN10x-R	Broadcom CSP
[3] Pkg Reflow Process Guidelines for Surface Mount Assemblies Application Note	PACKAGING-AN10X-R	Broadcom CSP
[4] Soldering Guidelines for Exposed Pad Die-Up Leadframe Packages Application Note	PACKAGING-AN20x-R	Broadcom CSP

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Functional Description

Overview

The Broadcom® B50612D is a single-chip Gigabit Ethernet (GbE) transceiver with Energy Efficient Ethernet™ (EEE) AutogrEEEn support that performs all of the physical layer (PHY) interface functions for 1000BASE-T, 100BASE-TX, and 10BASE-T Ethernet on Category 5 unshielded twisted-pair (UTP) cabling. The 10BASE-T operation is supported on Category 3, 4, and 5 UTP cabling. The B50612D connects to a Media Access Controller (MAC) or switch controller through an RGMII interface.

The device connects directly to the twisted-pair wiring of the network (through isolation transformers) on the other side. The B50612D is designed to be fully compliant with the IEEE 802.3™ standard. It can be programmed to auto-negotiate its operating speed and duplex mode based on the capabilities of the link partner and the quality of the cabling plant.

The B50612D device adheres to Broadcom's quality procedures and meets or exceeds the performance and functionality tested as part of our comprehensive product characterization, qualification, and functional verification process.

Modes of Operation

The B50612D operates in RGMII-to-copper (10/100/1000BASE-T) mode.

In the 48-pin MLP package, when TEST3/TEST2 = 00 or 11, and LED4 is external pulled-down, LED3 is sampled as MODE_SEL[1] and LED2 is sampled as MODE_SEL[0] during reset.

See “48-Pin MLP Package Hardware Configuration” on page 60 for details.

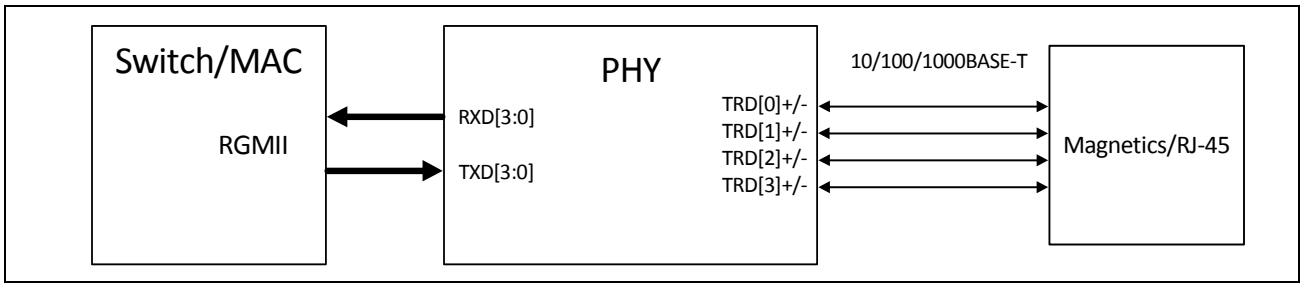
For the 48-pin MLP package, MODE_SEL[1:0] can also be configured using register 1Ch shadow value 01011 bits [4:3] after reset.

Table 1: RGMII Mode Selection by Hardware

MODE_SEL[1]	*MODE_SEL[0]*	*Function*
0	0	RGMII 3.3V
0	1	RGMII 2.5V
1	0	RGMII HSTL (1.8V)
1	1	RGMII 3.3V

A block diagram of a typical application is shown in Figure 2.

Figure 2: Typical RGMII-to-10/100/1000BASE-T Application



Reduced Gigabit Media Independent Interface

The Reduced Gigabit Media Independent Interface (RGMII) is a subset of the Gigabit Media Independent Interface (GMII), which allows the MAC with a reduced pin count to connect to the PHY. Compared to GMII, the number of data signal pins required to and from the MAC is reduced to half by clocking data on both the rising and falling edge of the transmit clock. This makes the RGMII digital data bit transmission rate effectively twice that of the GMII, while the clock speed remains the same. The RGMII and GMII interfaces use the same hardware and internal circuitry, though only TXD[3:0] and RXD[3:0] signals are used in RGMII mode. For information about this mode, see "RGMII Interface" on page 56.

Management Interface

The B50612D contains a large set of management registers. The Status and Control registers of the B50612D are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz. The management interface supports the defined Status and Control registers of IEEE 802.3 Clauses 22, 28, 37, and 40. In addition, the B50612D contains multipurpose registers for extended software control.

Encoder

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs preequalization for 100m of Category 3 cabling. In 100BASE-TX mode, the B50612D transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in "Stream Cipher" on page 29. The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the B50612D simultaneously transmits and receives a continuous data stream on all 4 pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the 4 twisted pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2 bytes of the preamble with a start-of-stream delimiter and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE standard 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHY.

Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the B50612D asserts the MII receive error (RX_ER) signal. RX_ER is also asserted when the link fails or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder.
- Descrambled.
- Translated back into byte-wide data.

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. The decoded data is driven onto the RGMII receive data pins. Decoding complies with IEEE standard 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHY.

Carrier Sense

In 1000BASE-T RGMII mode, the carrier sense information is encoded into the control signals. For details, see “Operational Description” on page 48. When Carrier Sense is asserted, the RGMII RX_DV pin is asserted [0,1] and RXD[3:0] pins are FF. For details, refer to the Reduced Gigabit Media Independent Interface (RGMII) specification.

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Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD± pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the link fail state and the transmission and reception of data packets are disabled. When a valid signal is detected on the receive pair for a minimum of 1 µs, the link monitor enters link-pass state and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 microsecond, the link monitor enters the link-pass state and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 µs, the link monitor enters the link-fail state and the transmission and reception of data packets are then disabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The B50612D achieves optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

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Crosstalk Canceler

The B50612D transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

Analog-to-Digital Converter

Each receive channel has its own 125 MHz Analog-to-Digital Converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25 MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other end is configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The B50612D automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high-frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation and thus reducing system complexity for routing and bill of materials.

Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bitwide linear feedback shift register (LFSR), producing a 2047-bit nonrepeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bitwide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remappings of the 33-bitwide LFSR output. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bitwide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The B50612D enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that interpacket gaps containing idles or frame extensions are received at expected intervals. When the B50612D detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the B50612D is forced into the link-fail state. In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

Wire Map and Pair Skew Correction

During 1000BASE-T operation, the B50612D has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the B50612D) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable
- Polarity errors caused by the swapping of wires within a pair

The B50612D also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The B50612D can tolerate delay skews of up to 64 ns. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100 Mbps operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

Automatic MDI Crossover

Note: This function only operates when the copper auto-negotiation is enabled.

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The B50612D can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the B50612D normally transmits on the TRD[0]± pin and receives on the TRD[1]± pin.

When connecting to another device that does not perform MDI crossover, the B50612D automatically switches its TRD± pin pairs, when necessary, to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the B50612D swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. During 100BASE-TX and 1000BASE-T operation, pair swaps automatically occur within the device and do not require user intervention.

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8/17/2016 RCXT3

10BASE-T/100BASE-TX Forced Mode Auto-MDIX

Note: This function only operates when the copper auto-negotiation is disabled.

This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for a least 4 seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100BASE-TX idles are detected. Once detected, the PHY returns to forced mode operation.

The user should set the same speed in register 0 and the auto-negotiation advertisement register 4.

> ***Example:*** To force 100BASE-TX full-duplex, write register 0 with 2100h and register 4 with 0181h. The feature is enabled by writing register 18h, shadow 7, bit 9 = 1. Copper link can be determined by reading register 19h, bit 2.

Auto-Negotiation

The B50612D negotiates its mode of operation over the copper media using the auto-negotiation mechanism, defined in the IEEE 802.3u and IEEE 802.3ab specifications. When the auto-negotiation function is enabled, the B50612D automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The B50612D can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex
- 100BASE-TX full-duplex and/or half-duplex
- 10BASE-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be enabled or disabled by hardware and software control, but is always required for 1000BASE-T operation. For details on auto-negotiation using Next Page Exchange, see “Next Page Exchange” on page 56.

Note: Refer to the *10/100/100BASE-T Linking Issues Application Note* (Reference [1] on page 23) for more details.

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8/17/2016 RCXT3

Ethernet@Wirespeed™

Ethernet@Wirespeed™ is an enhancement to auto-negotiation that allows a network connection even over impaired cable plants. If a link cannot be established at the highest common denominator within a programmable number of link attempts, then the B50612D advertises the next highest advertised speed using auto-negotiation. Below is an example of how Ethernet@Wirespeed works.

At startup, the B50612D is advertising 1000BASE-T, 100BASE-TX, and 10BASE-T capabilities per registers 04h and 09h, and the Link Partner is also advertising the same capabilities:

- If a link cannot be established within a programmable number of link attempts (two to nine) with 1000BASE-T being advertised, then an Ethernet@Wirespeed downgrade occurs, the 1000BASE-T capability is masked out on the B50612D, and the next highest advertised capability (100BASE-TX) is advertised.
- If a link cannot be established within a programmable number of link attempts (two to nine) with 100BASE-TX being advertised, then an Ethernet@Wirespeed downgrade occurs, the 100BASE-TX is masked out on the B50612D, and the next highest advertised capability (10BASE-T) is advertised.
- If a link cannot be established within a programmable number of link attempts (two to nine) with 10BASE-T being advertised, then an Ethernet@Wirespeed downgrade occurs and all advertising capabilities are enabled (1000BASE-T, 100BASE-TX, and 10BASE-T) on the B50612D and the whole process begins again. The B50612D has a link-up timer that times how long the link has been up. The link-up timer range is between 1.76 seconds to 2.68 seconds. If the link stays up longer than the link-up timer range, then the number of failed link attempts get reset to zero and the B50612D advertises the highest speed when it tries to establish link. The purpose of the link-up timer is to prevent scenarios where the link never gets established at a lower speed because the link at the higher speed is unstable and is going up and down quickly. In this situation, if the link stays up for less than the link-up timer range, the number of link failed attempts gets incremented and the B50612D tries to establish link at a lower speed.

The link-up timer can be bypassed by setting register 18h, shadow 7h, bit 10 = 1. Setting this bit causes the number of failed link attempts to get reset to zero after every link up condition, no matter how short the link up time is.

In addition, Ethernet@Wirespeed downgrade can be removed by any of the following events:

- Stable link-up condition for greater than 5 seconds.
- Unplug cable (no energy) greater than 1 second.
- Hardware reset
- Software reset (reg. 00h, bit 15 = 1)
- Disable auto-negotiation (reg. 00h, bit 12 = 0)
- Restart auto-negotiation (reg. 00h, bit 9 = 1)
- Disabling Wirespeed (reg. 18h, shadow 7h, bit 4 = 0)
- Auto-negotiation resolves to no Highest Common Denominator (HCD)
- Programmable (2 to 5) fails of the lowest supported speed wraps back to the original highest advertised speed.

Note: The number of failed link attempts before downgrading to a slower speed is programmable. The number can be programmed anywhere from two to nine failed link attempts before downgrading to a lower speed. The default value is five failed link attempts. See "Changing the Number of Failed Link Attempts Before Ethernet@Wirespeed Downgrade" for more details.

Software Disable

Disabling Ethernet@Wirespeed is done by writing register 18h, shadow 7h, bit 4 = 0.

Changing the Number of Failed Link Attempts Before Ethernet@Wirespeed Downgrade

The number of failed link attempts before downgrading to a slower speed is programmable.

The number can be programmed anywhere from two to nine failed link attempts before downgrading to a lower speed. The default value is five failed link attempts. The number of failed link attempts before downgrading to a lower speed can be programmed by writing to register 1Ch, shadow 4h, bits[4:2] as shown in Table 2 on page 33.

Table 2: Changing the Number of Failed Link Attempts before Downgrade

Bits[4:2]	*Description*
000	Number of failed link attempts before Ethernet@Wirespeed downgrade = 2
001	Number of failed link attempts before Ethernet@Wirespeed downgrade = 3
010	Number of failed link attempts before Ethernet@Wirespeed downgrade = 4
011	Number of failed link attempts before Ethernet@Wirespeed downgrade = 5 (Default Value)
100	Number of failed link attempts before Ethernet@Wirespeed downgrade = 6
101	Number of failed link attempts before Ethernet@Wirespeed downgrade = 7
110	Number of failed link attempts before Ethernet@Wirespeed downgrade = 8
111	Number of failed link attempts before Ethernet@Wirespeed downgrade = 9

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8/17/2016 RCXT3

Monitoring Ethernet@Wirespeed

The status of the Ethernet@ Wirespeed downgrade can be monitored through the following registers and LEDs:

- Ethernet@Wirespeed downgrade status (register 11h, bit 14)
- Ethernet@Wirespeed downgrade ([register 1Dh, bit 15 = 1], bit 12)
- Ethernet@Wirespeed disable Gigabit advertising ([register 1Dh, bit 15 = 1], bit 14)
- Ethernet@Wirespeed disable 100BASE-TX advertising ([register 1Dh, bit 15 = 1], bit 13)
- HCD status ([Register 1Dh, bit 15 = 1], bits[11:0])
- Auto-negotiation HCD and current status (register 19h, bits[10:8])
- Ethernet@Wirespeed downgrade LED on LED1 (register 1Ch, shadow 0Dh, bits[3:0] = 1001
- Ethernet@Wirespeed downgrade LED on LED2 (register 1Ch, shadow 0Dh, bits[7:4] = 1001

Energy Detect

The energy-detect feature provides an output signal (EnergyDetect) indicating the presence or absence of energy being received on the copper analog input pins of the chip. Additionally, the copper energy-detection status can be monitored from register 1Ch, shadow 11111, bit 5. See “Operational Description” on page 48 for details.

Internal Voltage Regulator

Control circuitry for voltage regulator has been provided for designs where 1.2V supply is not available. The circuits allow sources at from 2.5V to 3.3V to be reduced to 1.2V. This regulator utilize internal dropping elements and do not require external components. See “Internal Voltage Regulator” on page 57 for details.

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8/17/2016 RCXT3

Power-Down Modes

Three low-power modes are supported in the B50612D:

- Ultra-low power-down mode (IDDQ-LP mode)
- IDDQ with Soft Recovery mode (IDDQ-SR mode)
- IDDQ with Signal Detect mode (IDDQ-SD mode)
- Standby power-down mode
- Auto power-down mode

For details, see "Auto Power-Down Mode" on page 50.

Additional power savings can be made by:

- Using 2.5V instead of 3.3V for OVDD
- Using external 1.2V supply rather than the internal regulator

Jumbo Packets

In copper mode, packets up to 10 KB in length can be supported with the following register writes:

- Register 18h, shadow 000, bit 14 = 1 (default = 0)
- Register 10h, bit 0 = 1 (default = 0)

Energy Efficient Ethernet

The B50612D contains support for Energy Efficient Ethernet. EEE is IEEE 802.3az, an extension of the IEEE 802.3™ standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both sides of a link to disable portions of each PHY's operating circuitry and save power.

The B50612D offers two basic modes of operation:

1. Native EEE mode for MACs that support LPI signaling across the RGMII interface and
2. AutogrEEEn mode for legacy MACs that do not support LPI signaling across the RGMII interface.

When in either Native or AutogrEEEn mode:

- The PHY supports 100BASE-TX Full duplex.
- The PHY supports 1000BASE-T Full duplex.
- Auto-Negotiation must be enabled.
- Link status does not change.
- Frames are not dropped nor corrupted.
- The transition time to and from the lower power levels are transparent to upper layer protocols and applications.

In addition to the standard EEE operation, the B50612D supports the following enhancements to the AutogrEEEn functions:

- Delayed Entry
- Fixed Latency
- Variable Latency

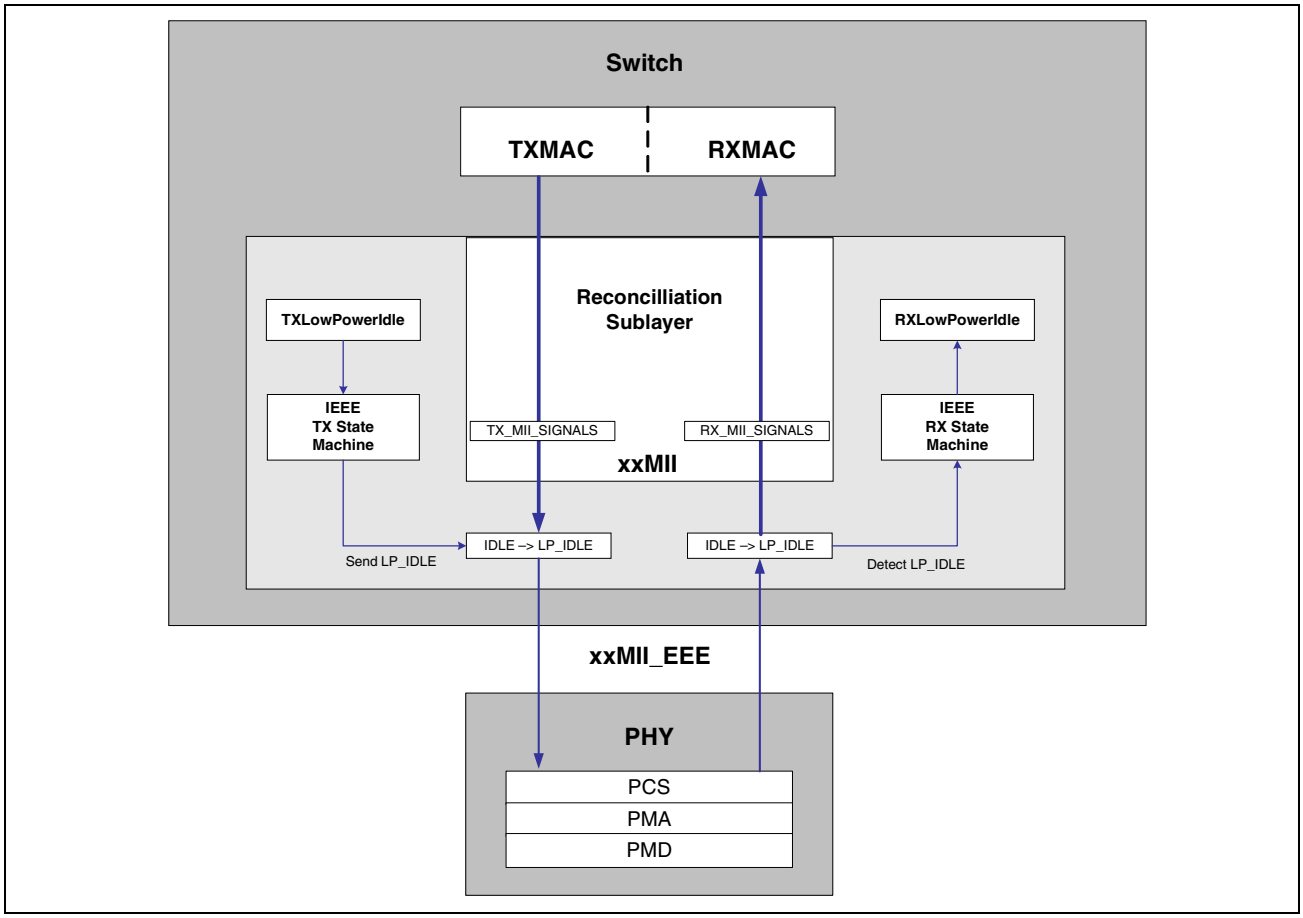
Native EEE Mode

Native EEE mode is used with MACs that support the IEEE 802.3az LPI code group signaling through the RGMII interfaces. Figure 3 shows LPI support in the MAC.

The MAC also has to be aware that the medium is not immediately available when in LPI mode. This means that the MAC must be able to:

- Hold off data transmission when link is in LPI mode.
- Account for wake-up time when transitioning from LPI to the Active state when it wants to initiate data transmission.
- Optionally support the IEEE 802.3AB protocol (LLDP), used by devices to negotiate additional wake-up times.

Figure 3: Native EEE Mode (Mac-Supported EEE LPI)



Native EEE Flow

The following steps show the procedure for activating Native EEE mode. By default, the Native EEE mode is enabled in the B50612D device:

1. Native EEE mode can be disabled or enabled through registers.
2. Advertise normal auto-negotiation capabilities:
   a. 10BASE-T and 100BASE-TX abilities: register 04h
   b. 1000BASE-T abilities: register 09h
3. Advertise EEE auto-negotiation capabilities:
   a. 100BASE-TX EEE ability: Clause 45 DEVAD 7.3Ch.1 = 1
   b. 1000BASE-T EEE ability: Clause 45 DEVAD 7.3Ch.2 = 1
4. Initiate auto-negotiation:
   a. Set restart auto-negotiation = 1: register 00, bit 12
   b. Local and remote PHY auto-negotiate speed, duplex, remote fault, pause, master/slave, next page and EEE abilities.
5. Link is established (10BASE-T, 100BASE-TX or 1000BASE-T).
6. The MAC looks at the EEE Resolution Status registers to determine what EEE speeds are supported:
   a. Read EEE 1000BASE-T resolution:
   – EEE_1000T_Resolution: Clause 45 DEVAD 7.803Eh.2 = 1
   b. Read EEE 100BASE-TX resolution:
   – EEE_100TX_Resolution: Clause 45 DEVAD 7.803Eh.1 = 1
7. If local and remote PHY support EEE then they can optionally negotiate longer system wake-up times (Tw_sys) through LLDP:
   a. The default settings below are used if LLDP is not used:
   – Tw_sys default for 100BASE-TX = 20.5 µs
   – Tw_sys default for 1000BASE-T = 16.5 µs
8. The MAC determines when the B50612D will transmit LPI signals on the MDI. The B50612D will start transmitting LPI signals when the B50612D receives the LPI code groups from the MAC as specified in IEEE 802.3az:
   a. If 100BASE-TX link is established, then the B50612D can start sending LPI.
   b. If 1000BASE-T link is established, then the B50612D will only enter LPI mode after it transmits LP_IDLE and receives LP_IDLE from the remote PHY.

Note: The B50612D communicates and coordinates the LPI transition across the MDI.

9. The B50612D keeps the link-related parameters up to date through refresh.
10. The MAC determines when the B50612D will stop sending LPI signals on the MDI and transition to normal mode. The B50612D will stop transmitting LPI signals when the B50612D receives normal interframe gap from the MAC as specified in IEEE 802.3az.

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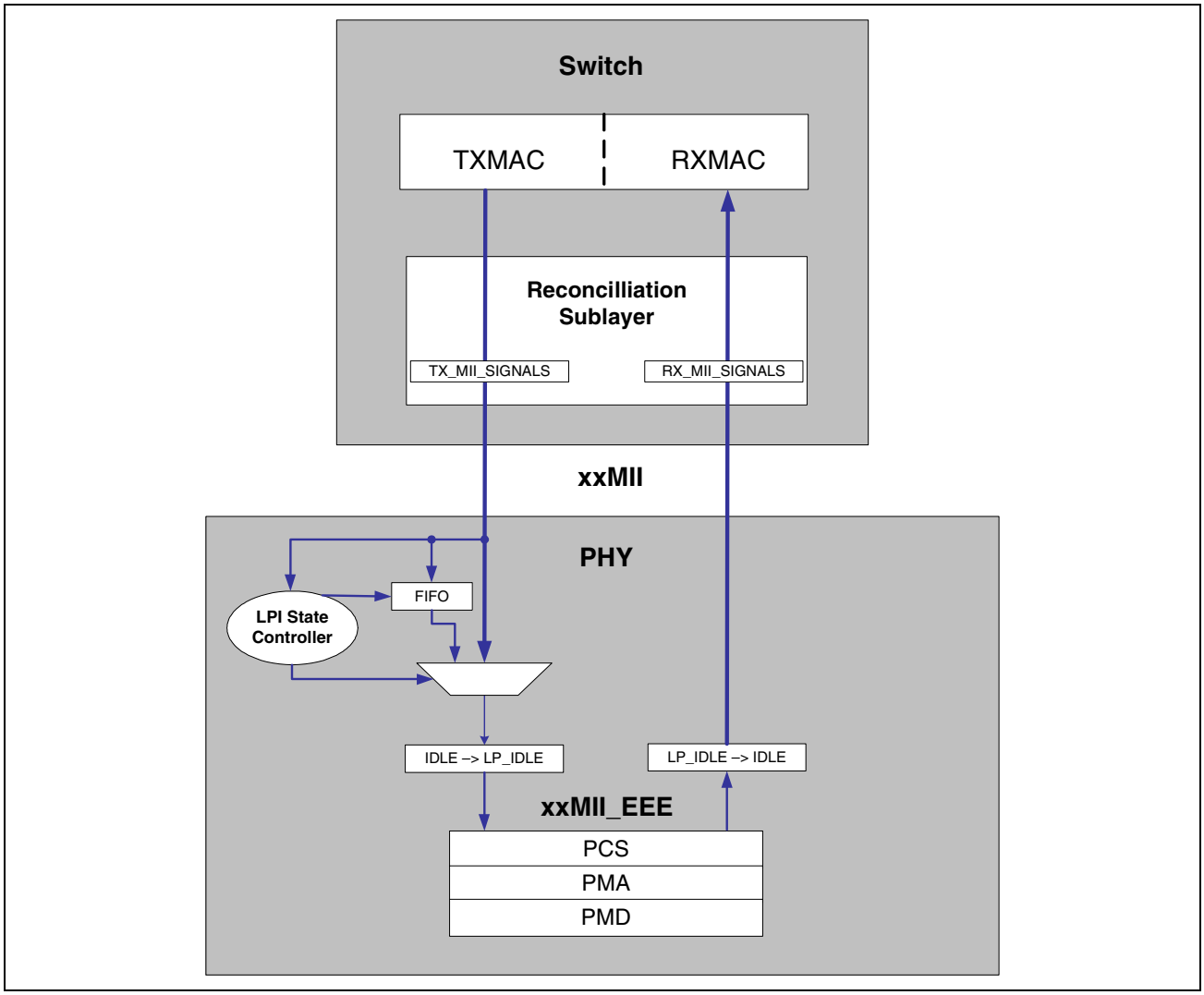
AutogrEEEn Mode

AutogrEEEn mode is used with legacy MACs that do not support the IEEE 802.3az LPI code group signaling through the GMII interfaces. Figure 4 shows LPI support in the PHY. AutogrEEEn mode transmits the same LPI signals on the MDI as Native EEE mode making it compatible with PHYs that support either Native EEE or AutogrEEEn mode.

AutogrEEEn mode has the following benefits:

- The MAC does not need to be aware that the PHY is transmitting LPIs.
- The MAC assumes that the media is always available to it.
- Allows use of all speeds and legacy MACs.

Figure 4: AutogrEEEn Mode (PHY-Supported EEE LPI)



AutogrEEEn Flow

By default, the AutogrEEEn mode is enabled in the B50612D device. It can also be controlled by registers:

1. To enable AutogrEEEN mode, set the Top-Level Expansion register 40h.0 = 1.
2. Advertise normal auto-negotiation capabilities:
   a. 10BASE-T and 100BASE-TX abilities: register 04h
   b. 1000BASE-T abilities: register 09h
3. Advertise EEE auto-negotiation capabilities:
   a. 100BASE-TX EEE ability: Clause 45 DEVAD 7.3Ch.1 = 1
   b. 1000BASE-T EEE ability: Clause 45 DEVAD 7.3Ch.2 = 1
4. Optionally enable Variable or Fixed Latency mode (see "Variable/Fixed Latency Modes" on page 40) by setting Variable_Latency_En: Top-Level Expansion register 40h.2 = 1
5. Initiate Auto-Negotiation:
   a. Set Restart Auto-Negotiation = 1: register 00h, bit 12
   b. Local and Remote PHY auto-negotiate Speed, Duplex, Remote Fault, Pause, Master/Slave, Next Page, and EEE abilities.
6. The link is established (10BASE-T, 100BASE-TX or 1000BASE-T).
7. The Mac looks at the EEE Resolution Status registers to determine what EEE speeds are supported:
   a. Read EEE 1000BASE-T Resolution
      EEE_1000T_Resolution: Clause 45 DEVAD 7.803Eh.2 = 1
   b. Read EEE 100BASE-TX Resolution
      EEE_100TX_Resolution: Clause 45 DEVAD 7.803Eh.1 = 1
8. The B50612D transmits LPI signals on the MDI when the number of consecutive idles is equal to the Wait_IFG_Length threshold:
   a. If 100BASE-TX link is established, the B50612D can start sending LPI.
   b. If 1000BASE-T link is established, the B50612D enters LPI mode only after it transmits LP_IDLE and receives LP_IDLE from the remote PHY.

Note: The B50612D communicates and coordinates the LPI transition across the MDI. See "MDI LPI Operation" on page 40.

9. The B50612D keeps link-related parameters up-to-date through refresh.
10. The B50612D stops sending LPI signals on the MDI and transitions to normal mode when a transmit data is received from the MAC.

MDI LPI Operation

In 100BASE-TX mode, the local PHY transmits a special LP_IDLE signal to communicate to the link partner that the local system is entering LPI mode. In 1000BASE-T mode, the transmit function of the local PHY enters a quiet mode only after the local PHY transmits LP_IDLE and receives LP_IDLE from the remote PHY. If the remote PHY does not signal LP_IDLE, then neither PHY can go quiet. The LPI requests are still passed from one end to the other end of the link.

There are three states visible above the EEE PHY when in Native EEE mode. For AutogrEEEn mode these states are handled by the B50612D:

- Active: Transmission of Data and Normal Idle
- Low Power Idle: Transmission of Low Power Idle (LPI)
- Hold: Transition state between Low Power Idle and Active

During LPI mode, only two states are visible: sleep and quiet. For times in each state and values, see Table 3.

Table 3: EEE Timing Parameters

	T_s (μsec)		T_q (μsec)		T_r (μsec)		T_{w_sys} (μsec)
Protocol	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***	***Default***
100BASE-TX	200	220	20000	22000	200	220	20.5
1000BASE-T	182	202	20000	24000	198	218.2	16.5

Variable/Fixed Latency Modes

When in AutogrEEEn mode, the B50612D supports either variable or fixed latency mode.

When operating in variable latency mode:

- Non-IDLE characters are written into the 2K FIFO.
- The FIFO drains as the IDLEs accumulate in the traffic profile.
- The FIFO is bypassed once it is empty.

When operating in fixed latency mode, IDLE characters are stuffed in the FIFO to maintain a constant latency value in the stream.

Section 2: Hardware Signal Descriptions

The following conventions are used in Table 5 on page 54:

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open drain output
- OT= Tristateable signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR= Sample on reset
- CS= Continuously sampled
- ST = Schmitt trigger

The following conventions are used to express the I/O types in Table 5 on page 54. The I/O pin type is useful in referencing the DC pin characteristics contained in "Electrical Characteristics" on page 153:

- XT = Crystal inputs/outputs pin type
- D = Digital pin type
- G = RGMII pin type
- A = Analog pin type
- PECL = Positive Emitter Coupled Logic

Note: Pin groups that are not found on a certain package are represented by an en dash (–). Refer to the *How to Design with the B50612D Design Guide Application Note* (Reference [2] on page 23) for additional information regarding the configurations and bypassing of the power supply pins.

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8/17/2016 RCXT3

Table 4: Hardware Signal Descriptions

48-Pin MLP	*Label*	*I/O Type*	*Description*
Media Connections			
14/15 18/17 20/21 24/23	TRD[0]± TRD[1]± TRD[2]± TRD[3]±	A	**Transmit/Receive Pairs.** In 1000BASE-T mode, differential data from copper media is transmitted and received on all four TRD± signal pairs. In auto-negotiation, 10BASE-T, and 100BASE-TX modes, the B50612D normally transmits on TRD[0]± and receives on TRD[1]±. Auto-MDIX operation can reverse the pairs. There is 50Ω internal termination on each pin, so no external termination is required. Since this device incorporates voltage driven DAC, it does not require magnetics center-tap supply. Instead, connect the magnetics center-tap to AC ground through individual 0.1 µF cap.
Clock			
8 7	XTALI XTALO	I/XT O/XT	**25 MHz Crystal Oscillator Input/Output.** A continuous 25 MHz reference clock must be supplied to the B50612D by connecting a 25 MHz crystal between these two pins or by driving XTALI with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected.
RGMII			
40	GTXCLK	I_{PD} G	**RGMII Transmit Clock.** 2.5/25/125 MHz input. This clock is continuously driven from the MAC. It is used to synchronize the transmit data in 1000BASE-T (RGMII) mode. In RGMII mode, the GTXCLK signals must be running and valid before the rising edge of the /RESET signal or copper establishing link.
39 38 37 36	TXD[0] TXD[1] TXD[2] TXD[3]	I_{PD} G	**Transmit Data Input.** Byte-wide transmit data is input synchronously to the RGMII Transmit Clock.
35	TX_EN	I_{PD} G	**Transmit Enable.** Active-high. When TX_EN is asserted, the data on the TXD pins is encoded and transmitted.
33	RXC	OT G	**Receive Clock.** 2.5/25/125 MHz output. This clock is recovered from the incoming analog waveforms and is used to synchronize the receive data outputs: 1000BASE-T mode; the clock is 125 MHz, byte-aligned on RXD[3:0]. 100BASE-TX mode; the clock is 25 MHz, nibble-aligned on RXD[3:0]. 10BASE-T mode; the clock is 2.5 MHz, nibble-aligned on RXD[3:0].
32 31 28 27	RXD[0] RXD[1] RXD[2] RXD[3]	OT G	**Receive Data Outputs.** Byte-wide receive data output synchronous with the receive clock.

Table 4: Hardware Signal Descriptions (Cont.)

48-Pin MLP	Label	I/O Type	Description
26	RX_DV	OT, G	**Receive Data Valid**. Active-high. RX_DV indicates that a receive frame is in progress and that the data present on the RXD output pins is valid.
48	MDC	I_{PD}, ST	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions.
47	MDIO	I/O_{PU}, D,ST	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
Mode			
41	PHYA[0]	I_{PD}, SOR	**PHY Address Selects.** Active-high. Sampled on reset. **Test Clock.** In the 48-pin MLP package, if TEST3/TEST2 = 01, PHYA[0] is used for the JTAG function. PHYA[0]=TCK. JTAG serial clock. **PHYA Mode.** In the 48-pin MLP package, if TEST3/TEST2 = 11, the PHY address is 11000 + PHYA[0]. This allows the chip to have PHY address of 00000, 00001, 11000, and 11001. See "48-Pin MLP Package Hardware Configuration" on page 60 for details.
46	$\overline{\text{RESET}}$	I_{PU}, CS, ST	**Reset.** Active-low, Schmitt Trigger Input. The B50612D requires a hardware RESET prior to normal operation. Configuration settings obtained via Hardware Strap Option pins are latched on the rising edge of RESET.
45	LED1	I_{PU}, O	**LED1.** Polarity determined at reset. See "Dual Input Configuration/ LED Output Function" on page 58 for details. This pin can be Programmed to alternate modes. See "General-Purpose LED Programmability" on page 59 for details. **Test Mode Select.** In the 48-pin MLP package, if TEST3/TEST2 = 01, LED1 is used for JTAG function and LED1 = TMS. JTAG mode select input.
44	LED2	I_{PU}, O	**LED2.** LED2 pin. This is a dual function pin. Polarity is determined at reset. See "Dual Input Configuration/LED Output Function" on page 58 for details. For programming to alternate modes, see "General-Purpose LED Programmability" on page 59 for details. If TEST3/TEST2 = 00 or 11, LED2 is sampled during reset as MODE_SEL[0] if the device is not configured in LOM-LED mode. **Test Data Input.** If TEST3/TEST2 = 01, LED2 is used for the JTAG function and LED2 = TDI. JTAG serial data input.

Table 4: Hardware Signal Descriptions (Cont.)

48-Pin MLP	Label	I/O Type	Description
43	LED3	I_{PU}, O	**LED3/LED4.** LED3 and LED4 are dual function pins. Polarity is determined at reset. See "Dual Input Configuration/LED Output Function" on page 58 for details. For programming to alternate modes, see "General-Purpose LED Programmability" on page 59 for more details. 48-pin MLP Hardware Configuration. In the 48-pin MLP package, set the copper advertisement to auto-negotiate 10/100/1000BASE-T by default. If TEST3/TEST2 = 00 or 11, LED3 is sampled as MODEL_SEL[1] and LED4 is sampled as LOM-LED mode. **Test Data Output.** If TEST3/TEST2 = 01, LED3 is used for JTAG function and LED3=TDO. JTAG serial data output. See "48-Pin MLP Package Hardware Configuration" on page 60 for details. **CLK125 Clock Output.** LED4 pin can be configured to a 125MHz clock output by register setting. Continuous 125 MHz output and generated off the PLL (phase lock to the XTAL input). This clock is powered by OVDD power. **Super-Isolate Mode.** When both LED1 and LED4 pins are low during reset, super-isolate mode is enabled by default.
42	LED4	I_{PU}, O, Od	
6	TEST2	I_{PD}	**Test Mode Enables.** Active-high. These pins must always be pulled low during normal operation. These pins are used by Broadcom for test purposes only. In the 48-pin MLP package, when TEST3/TEST2 = 01, enable JTAG mode; LED1, LED2, LED3, and PHYA[0] are used for TMS,TDI,TDO, and TCK. If TEST3/TEST2 = 11, the PHY address is 11000 + PHYA[0]. This allows the chip to have PHY address of 00000, 00001, 11000, and 11001. See "48-Pin MLP Package Hardware Configuration" on page 60 for details.
5	TEST3	CS	
RDAC Bias			
10	RDAC	B	**DAC Bias Resistor.** Adjusts the reference current of the transmitter digital-to-analog converter. A 1.24 kΩ ±1% resistor is connected between the RDAC pin and GND

Table 4: Hardware Signal Descriptions (Cont.)

48-Pin MLP	*Label*	*I/O Type*	*Description*
Regulator			
4	REGSUPPLY	PWR	**Regulator supply input.** 2.5V to 3.3V input.
3	REGOUT	PWR	**Regulator output.** 1.2V.

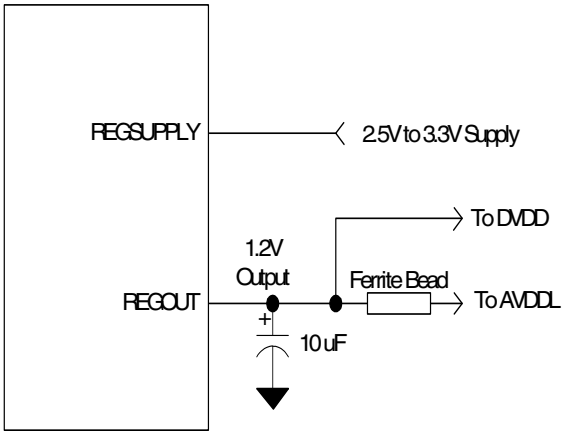


Table 4: Hardware Signal Descriptions (Cont.)

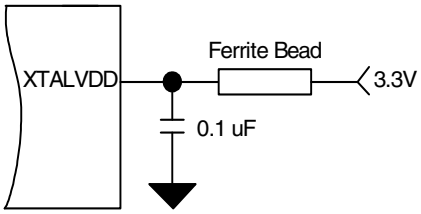
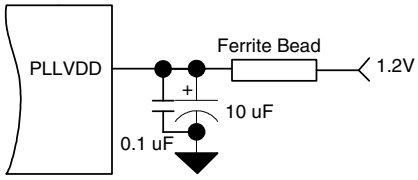
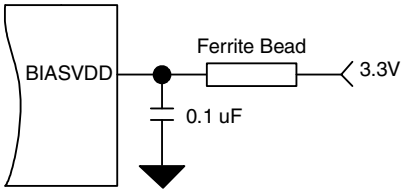
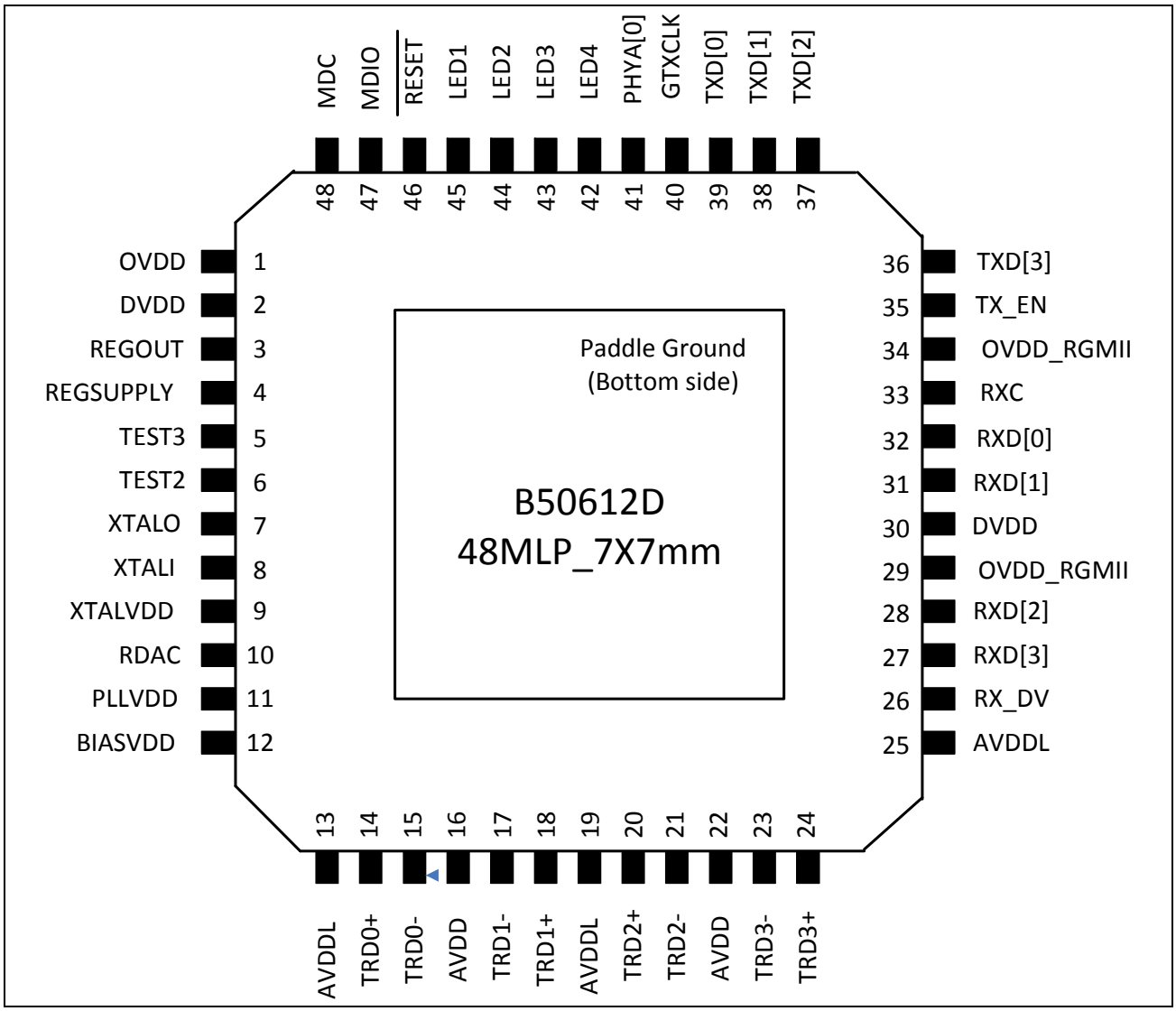
48-Pin MLP	Label	I/O Type	Description
29, 34	OVDD_RGMII	PWR	1.8V for HSTL mode; 2.5V or 3.3V for RGMII pads
1	OVDD	PWR	2.5V or 3.3V for non-RGMII pads
2, 30	DVDD	PWR	1.2V power for digital core
13, 19, 25	AVDDL	PWR	1.2V power for analog core
16, 22	AVDD	PWR	3.3V power for analog core
9	XTALVDD	PWR	3.3V crystal supply 
11	PLLVDD	PWR	1.2V PLL supply 
12	BIASVDD	PWR	**Bias VDD.** +3.3V. Normally filtered with a low resistance ferrite bead such as a Murata BLM11A601S or equivalent, as well as a 0.1 µF capacitor. 
Paddle Ground	GND	GND	Paddle ground

Figure 5: B50612D 48-Pin MLP Pinout Diagram, Top View



Section 3: Operational Description

RESET

The B50612D provides a hardware reset pin, $\overline{\text{RESET}}$, that resets all internal nodes to a known state. The reset pin must be asserted for at least 2.0 µs. Hardware reset should always be applied to the B50612D after power-up.

The B50612D also has a software reset capability. To enable the software reset, a 1 must be written to bit 15 of the MII Control register (address 00h). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if 0 is written to this bit.

The B50612D supports a soft-reset feature. If enable this function, set PHY register 00h bit 15 value of “1” will be a soft reset. This soft reset will reset everything expect for the MDIO registers. The feature is OFF by default and must be enabled by setting register 1Ch, shadow value 01011, bit 6 = 1. After enabling the soft-reset function, the PHY register 00h bit15 will not be able to self clear. Write a 0 to bit 15 of the MII Control register (address 00h) to clear it after software reset.

Mode pins that are labelled sample on reset (SOR) are latched during hardware reset. Similarly, software resets also latch new values for some SOR mode pins, except for those pins that contain LED functions. SOR mode pins that contain LED functions during normal operation retain the values latched during the previous hardware reset.

During reset, the PHY output pins connected to MAC are driven low.

PHY Address

The B50612D allows a unique PHY address for MII management. The address is set through the logic value of the PHYA[0] pin latched during reset. The PHY checks each MII management read or write command on its MDIO pin and performs the operation only if the address in the command matches the latched PHY address stored in the device.

Isolate Mode

The B50612D can be isolated from the RGMII MAC interface by writing a 1 to bit 10 of the Table 26 on page 73. When the transceiver is put into isolate mode, all RGMII MAC inputs are ignored, and all RGMII MAC outputs are tristated. While in isolate mode, the PHY still sends out link pulses or FLPs, depending on whether the PHY was configured for forced or auto-negotiation mode. A link is established if the link partner is forced or is advertising the same technologies. The MII management pins (MDC and MDIO), along with the MII registers, operate normally. Alternatively, setting bit 10 of the Table 26 on page 73 puts the transceiver in isolate mode. In either case, clearing the same bit removes the device from Isolate mode.

The B50612D can also be put into super-isolate mode by writing to register 18h, shadow value 010, bit 5 = 1. Super-isolate mode tristates the RGMII outputs, ignores the RGMII input signals, and disables the transmission of copper link pulses. This mode is useful when the B50612D needs to coexist with another PHY on the same adapter card, where only one PHY is active. Unlike the Isolate mode, the super-isolate mode is available only when the B50612D device is in the copper mode.

Standby Power-Down Mode

The B50612D can be placed into standby power-down mode using software commands. In this mode, all PHY functions, except the serial management interface and CLK125 output, are disabled. To enter standby power-down mode, set "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 73, bit 11 = 1. There are three ways to exit this mode:

- Clear MII Control register (address 00h), bit 11 = 0.
- Set the software reset bit 15, MII Control register (address 00h).
- Assert the hardware $\overline{\text{RESET}}$ pin.

Reads or writes to any MII register other than MII Control register (address 00h) while the device is in the standby power-down mode may cause unpredictable results. Upon exiting standby power-down mode, the B50612D remains in an internal reset state for 40 µs, and then resumes normal operation. When clearing the "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 73 bit 11 = 0, the internal reset state does not reset the writable MII management registers.

Auto Power-Down Mode

The B50612D can be placed into auto power-down mode to reduce chip power when the signal from the copper link partner is not present. Auto power-down mode works whether the device has copper auto-negotiation enabled or disabled. This mode is enabled by setting "Auto Power-Down Register (Address 1Ch, Shadow Value 01010)" on page 125, bit 5 = 1. However, when the B50612D is in forced 10 or 100 mode, the "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111)" on page 106, bit 9 should be set to 1. When auto power-down mode is enabled, the B50612D automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the B50612D is in Auto Power-down mode, it wakes up after 2.7s or 5.4s (determined by bit 4 of "Auto Power-Down Register (Address 1Ch, Shadow Value 01010)" on page 125) and sends link pulses while monitoring for energy from the link partner. The B50612D enters normal operation and establishes a link if energy is detected, otherwise, wake-up mode continues for a duration of 84 to 1260 ms. This is determined by the timer bits [3:0] of "Auto Power-Down Register (Address 1Ch, Shadow Value 01010)" on page 125 before going back to low-power mode.

Additional power savings can be realized by disabling the DLL by writing to "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)" on page 120, bit 1 = 0. This automatically disables the DLL when energy is lost. The DLL is automatically enabled during wake-up or when energy is detected. Do not enable this mode if the CLK125 signals are used by a MAC that needs a continuously running clock source.

TXC and RXC outputs can be disabled during auto power-down by setting the "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)" on page 120, bit 8 =1.

CLK125 Clock Output

A 125 MHz output clock is generated by the B50612D device from a 5× PLL using the 25 MHz clock at XTALI as a reference. The 125MHz clock should be used only when in RGMII mode to drive the MAC/Switch which cannot be used as RGMII RXC or GTXCLK clocks. The clock output remains active when the power-down bit (bit 11) in the 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h) is set.

In the 48-pin MLP package, the CLK125 is disabled by default. The B50612D can enable CLK125 to the LED4 pad by setting the Top- Level Expansion Register 34h: Spare Register 0, bit 1 = 1.

There are two ways to disable the CLK125 output:

- Power down the DLL as described in "Auto Power-Down Mode" on page 50.
- Clear the Top- Level Expansion Register 34h: Spare Register 0, bit 1 = 0.

Note: To use CLK125 for switch/MAC, contact local FAE or Broadcom engineer for details.

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Ultra-Low Power-Down Mode (IDDQ-LP Mode)

The B50612D can be placed into the ultra-low power-down mode (IDDQ), consuming the lowest power possible while voltage is being supplied to the device. This mode is especially useful for saving battery life in laptop designs when the user does not require a network connection.

Use the following methods to enter and exit the ultra-low power-down mode:

- To enter ultra-low power-down mode (software method), write to register 1Ch, shadow value 01100, bit 0 = 1.
- To exit ultra-low power-down mode (48-pin MLP), issue a hardware reset by forcing the $\overline{\text{RESET}}$ pin low. See Table 86 on page 148 for reset timing information.

Note: If B50612D enters ultra-low power-down mode by writing register 1Ch, shadow value 01100, bit 0 =1, the only way to exit ultra-low power-down mode is by issuing a hardware reset.

IDDQ with Soft Recovery (IDDQ-SR Mode)

B50612D provides an IDDQ mode that can disable IDDQ by register setting, which names IDDQ-SR mode.

Use the following settings to enter and exit the IDDQ-SR mode:

- To enter IDDQ-SR mode by using following setting in sequence:
  - Enable Standby Power-Down mode first, set Register 00h, bit [11] = 1.
  - Then, Set Register 1Ch to B021h. (Register 1Ch, shadow value 01100, bit [5,0] = 11).
- To exit IDDQ-SR mode by using following three ways:
  - Disable IDDQ-SR mode function in sequence:
  – Set Register 1C to B000h. (Register 1Ch, shadow value 01100), bits[5,0] = 00.
  – Disable Standby Power-Down mode, clear Register 00h, bit [11] = 0.
  - Set the software reset bit 15 = 1, MII Control Register (address 00h).
  - Issue a hardware reset.

IDDQ with Soft Recovery (IDDQ-SD Mode)

B50612D provides an IDDQ mode with Signal Detect supporting which names IDDQ-SD mode. During this mode, B50612D can use Signal Detect pin to inform CPU when copper energy is detected.

Use the following settings to enter and exit the IDDQ-SD mode:

- To enable IDDQ-SD mode by using following setting in sequence:
  - Enable Energy Detect function on $\overline{\text{INTR}}$ pin by set Register 1Ch to 900Eh (Register 1Ch, shadow value 04h, bit [1] = 1).
  - Enable Standby Power-Down mode, set Register 00h, bit [11] = 1.
  - Set Register 1Ch to B021h (Register 1Ch, SV 0Ch, bit [4] = 1).
- To exit by using the following three ways:

- Disable IDDQ-SD mode function in sequence:

– Set Register 1C to B000h (Register 1Ch, SV 0Ch), bit [4] = 0).

– Disable Standby Power-Down mode, clear Register 00h, bit [11] = 0.

- Set the software reset bit 15 = 1, MII Control Register (address 00h).
- Issue a hardware reset.

Reset Requirements

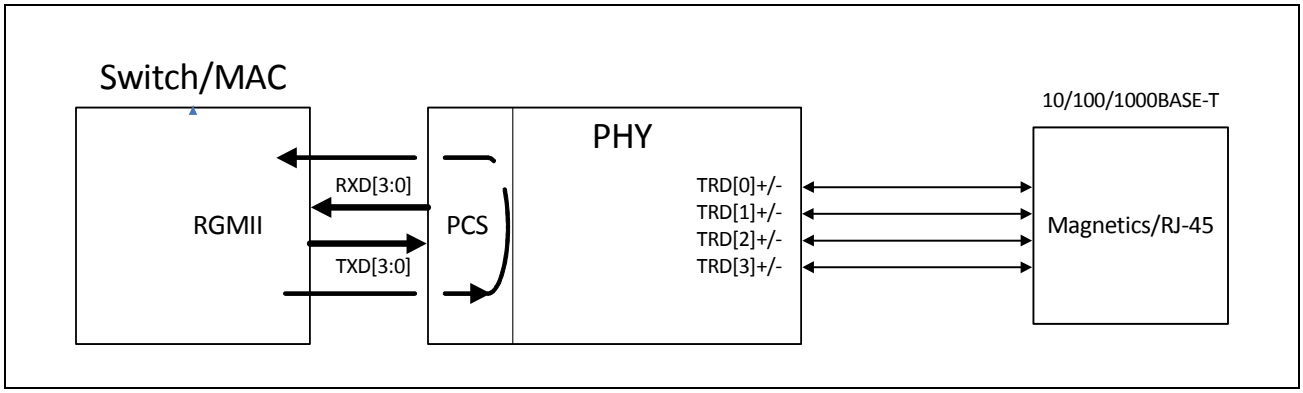
At least one hardware reset is required before entering IDDQ mode to ensure that the B50612D is properly configured before going into IDDQ mode.

Note: After exiting IDDQ mode, normal operation can be resumed following either a hardware or software reset of the chip. The software reset can be used only if a hardware reset has been done at least once since power was applied to the B50612D.

Internal Loopback Mode

All packets sent through the RGMII TXD pins are looped back internally to the RGMII RXD pins. The transmitter outputs TRD± are set to high impedance, and incoming packets on the cable are ignored. Loopback mode can be entered by writing a 1 to bit 14 of the MII Control register (Address 00h). To resume normal operation, bit 14 of the MII Control register must be 0.

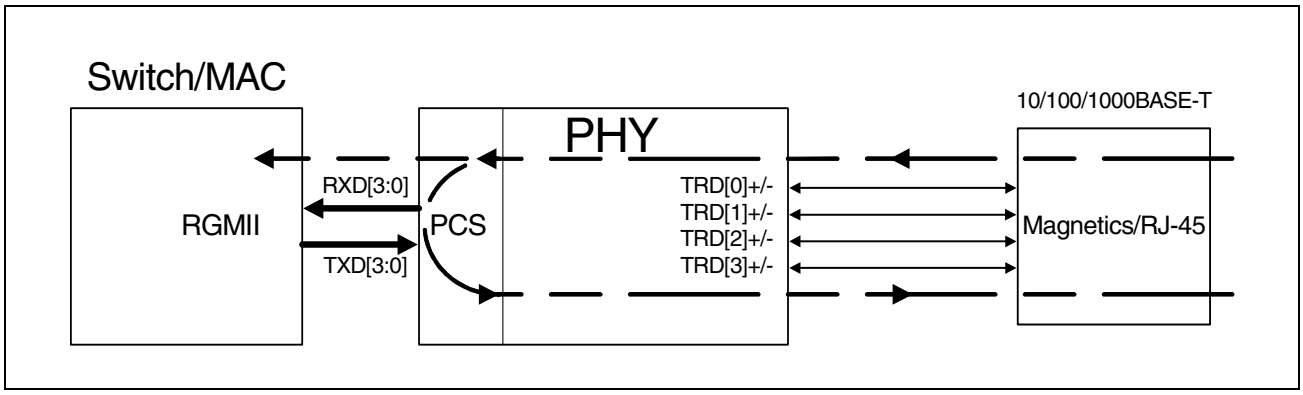
Figure 6: Internal Loopback Mode



Lineside (Remote) Loopback Mode

Lineside loopback mode allows the testing of the copper MDI interface from the link partner. This mode is enabled by setting bit 15 of the "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register (Address 18h, Shadow Value 100)" on page 105.The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the MAC interface. The MAC interface can be tristated by setting bit 11 of the "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register (Address 18h, Shadow Value 100)" on page 105.

Figure 7: Lineside (Remote) Loopback Mode

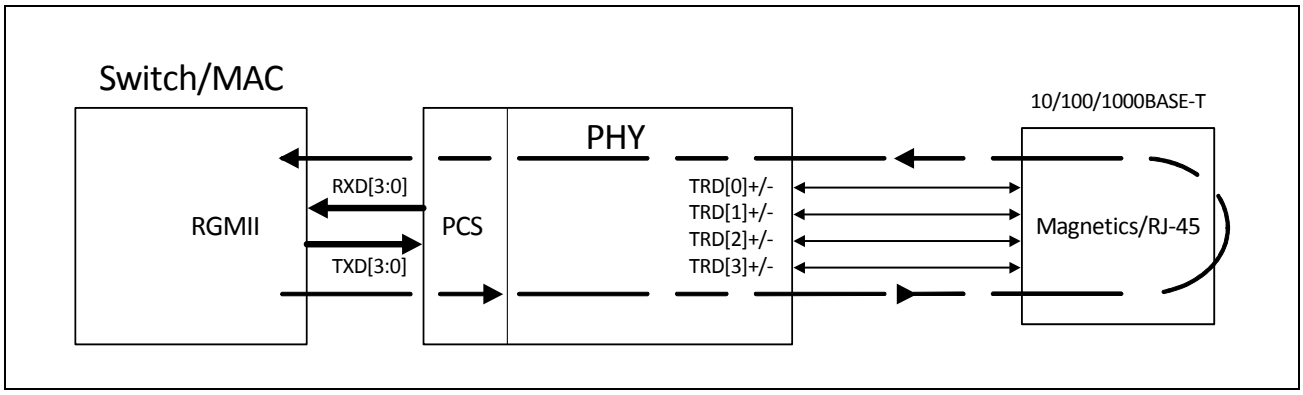


External Loopback Mode

The External Loopback mode allows in-circuit testing of the B50612D as well as the transmit path through the magnetics and the RJ-45 connector. External Loopback can be performed with or without a jumper block. External loopback using a jumper block tests the path through the magnetics and RJ45 connector. External loopback without the jumper block, only tests the B50612D's transmit and receive circuitry. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a jumper block must be inserted into the RJ-45 connector to support external loopback. The jumper block should have the following RJ-45 pins connected together:

1————————3
2————————6
4————————7
5————————8

Figure 8: External Loopback Mode



The following tables describe how the external loopback is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a jumper block.

Table 5: 1000BASE-T External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 1800h to register 09h	Enable 1000BASE-T Master mode
Write 0140h to register 00h	Enable Force 1000BASE-T
Write 8400h to register 18h	Enable External Loopback mode with external loopback plug

Table 6: 1000BASE-T External Loopback Without External Loopback Plug

Register Writes	*Comments*
Write 1800h to register 09h	Enable 1000BASE-T Master mode
Write 0140h to register 00h	Enable Force 1000BASE-T
Write 0014h to register 18h	Enable External Loopback mode without external loopback plug
Write 8400h to register 18h	Enable External Loopback mode

Table 7: 100BASE-TX External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 2100h to register 00h	Enable Force 100BASE-TX Full-Duplex mode
Write 8400h to register 18h	Enable External Loopback mode with external loopback plug

Table 8: 100BASE-TX External Loopback Without External Loopback Plug

Register Writes	*Comment*
Write 2100h to register 00h	Enable force 100BASE-TX full-duplex mode
Write 0014h to register 18h	Enable external loopback mode without external loopback plug

Table 8: 100BASE-TX External Loopback Without External Loopback Plug (Cont.)

Register Writes	Comment
Write 8400h to register 18h	Enable external loopback mode

Table 9: 10BASE-TX External Loopback With External Loopback Plug

Register Writes	Comments
Write 0100h to register 00h	Enable force 10BASE-T full-duplex mode
Write 8400h to register 18h	Enable external loopback mode with external loopback plug

Table 10: 10BASE-T External Loopback Without External Loopback Plug

Register Writes	Comments
Write 0100h to register 00h	Enable force 10BASE-T full-duplex mode
Write 0014h to register 18h	Enable external loopback mode without external loopback plug
Write 8400h to register 18h	Enable external loopback mode

Note: To exit the external loopback mode, Broadcom recommends a software or hardware reset.

Full-Duplex Operation

The B50612D supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable.

When auto-negotiation is disabled, full-duplex operation can be enabled by setting bit 8 of the "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)" on page 73.

When auto-negotiation is enabled, the full-duplex capability is advertised for:

- 10BASE-T when bit 6 in the "1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)" on page 79 is set.
- 100BASE-TX when bit 8 in the "1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)" on page 79 is set.
- 1000BASE-T when bit 9 in the "1000BASE-T Control Register (Address 09h)" on page 87 is set.

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Master/Slave Configuration

In 1000BASE-T mode, the B50612D and its link partner perform loop timing. One end of the link must be configured as the timing master and the other end as the slave, as defined by IEEE 802.3ab. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. However, if both partners are configured with identical repeater/DTE settings, each will generate an 11-bit random seed. The partner with the higher seed is configured as the master. If the local PHY and the link partner happen to generate the same random seed, auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave) or the random seeds match seven consecutive times, the B50612D sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register, and auto-negotiation is restarted.

Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the B50612D and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the B50612D is configured to advertise 1000BASE-T capability.

The B50612D also supports software controlled Next Page exchanges. When bit 15 of Table 29 on page 79 is written to a 1, all Next Page transactions are controlled through the MII management interface. This includes the three 1000BASE-T Next Pages, which are always sent first. The B50612D automatically generates the appropriate message code field for the 1000BASE-T pages. When the B50612D is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the B50612D is not configured to advertise 1000BASE-T capability and bit 15 of the "1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)" on page 79 is 0, the B50612D does not advertise Next Page ability.

RGMII Interface

The B50612D can communicate with Ethernet MACs through a reduced-pin-count Gigabit MII known as RGMII. This interface reduces the number of MAC signal pins by half with respect to GMII. Transmit and receive data are transferred on both edges of the GTXCLK and RXC clocks, respectively. The GTXCLK and RXC clock rates are:

- 125 MHz for 1000 Mbps data
- 25 MHz for 100 Mbps data
- 2.5 MHz for 10 Mbps data

Data is sent with the least significant nibble first. In the 48-pin MLP package, the RGMII mode can be changed by hardware or software. See "External Control 1 Register" on page 126 for an explanation of hardware-enabled settings.

To enable by software, write register 1Ch, shadow 01011, bits [4:3]. See "External Control 1 Register" on page 126.

While in copper mode, the RGMII receive timing can be adjusted, if needed, by software control. The RXD-to-RXC skew time can be delayed by approximately 1.9 ns by setting bit 8 of register 18h, shadow value 111.

The RGMII transmit timing can be adjusted, if needed, by software or hardware control. The TXD to GTXCLK delay time can be increased by approximately 1.9 ns by setting bit 9 of register 1Ch, shadow value 00011. Using these timing adjustments, the board designer can eliminate the need for board delay traces required by the RGMII specification.

Table 11: RGMII Transmit Data

RGMII Signal	*Signal Latched at GTXCLK Rising Edge*	*Signal Latched at GTXCLK Falling Edge*
TX_EN	TX_EN	TX_EN (XOR) TX_ER
TXD[3]	TXD[3]	TXD[7]
TXD[2]	TXD[2]	TXD[6]
TXD[1]	TXD[1]	TXD[5]
TXD[0]	TXD[0]	TXD[4]

Table 12: RGMII Receive Data

RGMII Signal	*Signal Latched at RXC Rising Edge*	*Signal Latched at RXC Falling Edge*
RX_DV	RX_DV	RX_DV (XOR) RX_ER
RXD[3]	RXD[3]	RXD[7]
RXD[2]	RXD[2]	RXD[6]
RXD[1]	RXD[1]	RXD[5]
RXD[0]	RXD[0]	RXD[4]

Internal Voltage Regulator

One voltage regulator is provided to ease power supply requirements for designs which may otherwise lack a 1.2V power supply. The regulator is internal and does not rely on external components.

The regulator output pin REGOUT automatically outputs 1.2V when REGSUPPLY is supplied with 2.5V to 3.3V.

When connected as described, the output pin REGOUT is brought out to allow filtering and power distribution.

Note: The regulator can supply a maximum of 200 mA.

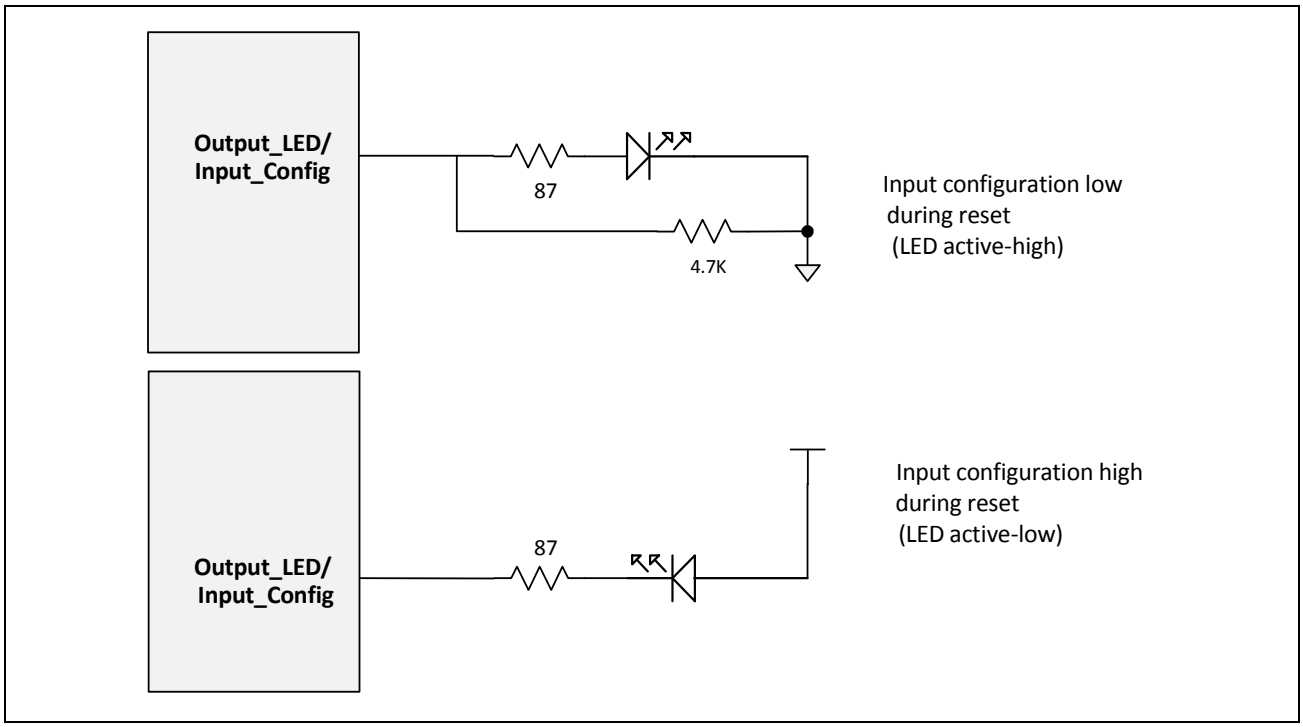
Dual Input Configuration/LED Output Function

All four LEDs pins have secondary functions. These pins serve as an input pin during the power-on/reset sequence. The logic level of the pin is sampled at reset and configures the secondary function. After the reset process is completed, the pin acts as an output LED during normal operation. The polarity of the output LED is determined based on the latched input value at reset. For example, if the value at the pin is high during reset, the LED output during normal operation is active low. The user must first decide, based on the individual application, the values of the input configuration pin shown in Table 13 on page 58 to provide the correct device configuration. The LED circuit must then be configured to accommodate either an active-low or active-high LED output (see Figure 9 on page 58).

Table 13: Dual Input Configuration/LED Outputs

LED Output (Normal Operation)	*Input Configuration Pin (Latched During Reset)*
LED4/LED3/LED2/LED1	See "48-Pin MLP Package Hardware Configuration" on page 60 for details.

Figure 9: LED Circuit for Dual Input Configuration/LED Output Pins



General-Purpose LED Programmability

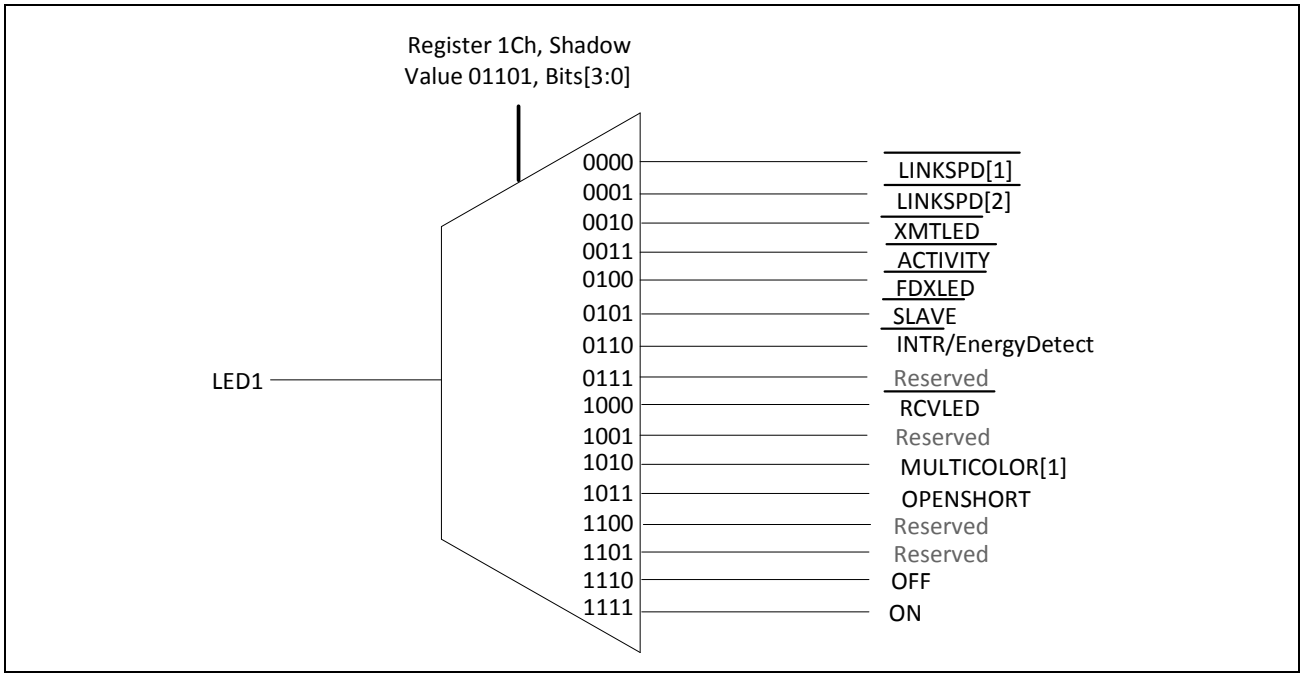
The B50612D has four LED pins that can be programmed to one of many useful LED functions. Four 4-bit control register words are provided to allow the user to select the LED function for each of the pins. These control words are located in register 1Ch, shadow value 01101 and shadow value 01110. Table 14 details each of the four programmable LEDs, their corresponding register bits, and default settings.

Table 14: Programmable LEDs

48-Pin MLP	*Pin Name*	*Register Bits*	*Default Value*	*Default Function*
45	LED1	Register 1C, shadow value 01101, bits [3:0]	0000	LINKSPD[1]
44	LED2	Register 1C, shadow value 01101, bits [7:4]	0001	LINKSPD[2]
43	LED3	Register 1C, shadow value 01110, bits [3:0]	0011	ACTIVITY
42	LED4	Register 1C, shadow value 01110, bits [7:4]	0110	$\overline{\text{INTR}}$

Each of the output functions exists as an internal device signal that is multiplexed to a given general-purpose LED pin when the corresponding register bits are written with the appropriate register value. Figure 10 is a graphical representation of the multiplexer functionality of the programmable LED and uses LED1 as an example.

Figure 10: Programmable LED Multiplexer



When LEDs are programmed to $\overline{\text{LINKSPD[1]}}$ and $\overline{\text{LINKSPD[2]}}$ function, it indicates the link and speed status of the copper interface as shown in Table 15 on page 60.

Table 15: LINKSPD[2:1] LED Function (Default-LED Mode/Non-LOM-LED Mode)

$\overline{\text{LINKSPD[2]}}$	***$\overline{\text{LINKSPD[1]}}$***	***Link/Speed***
0	0	Linked @ 1000BASE-T
0	1	Linked @ 100BASE-TX
1	0	Linked @ 10BASE-T
1	1	No link

Note: 0 means LED is turned on.

48-Pin MLP Package Hardware Configuration

Test pins TEST3/TEST2 can be used to set the B50612D to enter three different modes: JTAG mode (test mode), normal operation mode, and PHYA mode.

JTAG Mode

When TEST3/TEST2 = 01, the device enters in a test mode where JTAG operations can be executed. In this mode, the following pins change their regular functions for the JTAG signal functions.

Table 16: 48-Pin MLP Active Pin Test Function in JTAG Mode

Pin Names	***Active Function***
LED3	TDO
LED2	TDI
LED1	TMS
PHYA[0]	TCK

Normal Operation Mode and PHYA Mode

When TEST3/TEST2 = 00 or 11, the device operates normally. In these two modes, several device parameters can be configured at startup using pins:

- PHY address
- Super-isolate mode select
- RGMII mode select
- LOM-LED mode

PHY Address

The physical address of the B50612D is determined by the voltage levels in PHYA[0] and TEST3/TEST2 pins. Table 17 on page 61 shows the four possible PHY addresses for the B50612D.

Table 17: 48-Pin MLP PHY Address Based on PHYA[0] and TEST3/TEST2 Settings

		TEST3/TEST2	
	–	00	11
PHYA[0]	0	00000	11000
	1	00001	11001

Super-Isolate Select

In the 48-pin MLP package, LED1 and LED4 are sampled during reset as super-isolate mode select, active-low, sampled on reset. When LED1 and LED4 pins are low during reset, super-isolate mode is enabled.

RGMII Mode

RGMII modes can be selected by setting LED3/LED2 during power on reset. Table 18 shows the various MAC interface (RGMII) modes available in the device.

Note: LED4 = 0.

Table 18: 48-Pin MLP RGMII Mode

LED3/LED2	MAC RGMII Mode
0 0	RGMII 3.3V
0 1	RGMII 2.5V
1 0	RGMII HSTL 1.8V
1 1	RGMII 3.3V

LOM-LED Mode

LOM-LED mode is a simplified LED reporting mode that uses LED2/LED1 to show the operating link signal rate. Table 19 shows the definition of LED link signal rate reporting. The LOM-LED can be enabled by pull-high LED4 during power on reset.

Table 19: 48-Pin MLP LOM-LED Link Signal Rate Reporting

LED2/LED1	MAC RGMII Mode
0 0	–

Table 19: 48-Pin MLP LOM-LED Link Signal Rate Reporting (Cont.)

LED2/LED1	MAC RGMII Mode
1 0	1G Link
0 1	100M Link
1 1	Others

This mode has two RGMII modes (voltage-level communicating with MAC) shown in Table 20.

Table 20: 48-Pin MLP RGMII Modes for LOM-LED Operation

LED3	MAC RGMII Mode
0	RGMII 3.3V
1	RGMII HSTL 1.8V

TEST and LED Configuration Matrix

Table 21 and Table 22 show the 48-pin MLP package TEST3/TEST2 and LEDs hardware configuration matrix.

Table 21: Using TEST3/TEST2 Pins to Set JTAG, Normal Operation, and PHYA Modes

TEST3/TEST2	JTAG Mode 01	Normal Operation 00		PHYA Mode 11	
LED4[ab]	–	1	0	1	0
LED3	TDO	MODE_SEL[1]	MODE_SEL[1]	MODE_SEL[1]	MODE_SEL[1]
LED2	TDI	–	MODE_SEL[0]	–	MODE_SEL[0]
LED1	TMS	–	–	–	–
PHYA[0]	TCK	PHYA[0]	PHYA[0]	11000 + PHYA[0]	11000 + PHYA[0]

a. LED4 is sampled during reset as LOM-LED mode, active-high. When LED4 is set to non-LOM-LED mode, LED2 will be MODE_SEL[0] function, active-high
b. LED1/LED4 are sampled during reset as Super-isolate mode, active-low. When LED1/LED4 are low during POR, enable Super-isolate mode by default.

Table 22: 48-Pin MLP Package RGMII Mode Selection

RGMII Mode	*MODE_SEL[1,0]*	*Pin Configuration*		
RGMII 3.3V	00	TEST3/TEST2 = 00 or 11	LED3 = 0	LED2 = 0	LED4 = 0
RGMII 2.5V	01	TEST3/TEST2 = 00 or 11	LED3 = 0	LED2 = 1	LED4 = 0
RGMII HSTL 1.8V	10	TEST3/TEST2 = 00 or 11	LED3 = 1	LED2 = 0	LED4 = 0
RGMII 3.3V	11	TEST3/TEST2 = 00 or 11	LED3 = 1	LED2 = 1	LED4 = 0
RGMII 3.3V	00	TEST3/TEST2 = 00 or 11	LED3 = 0	LED2 = X[a]	LED4 = 1
RGMII HSTL 1.8V	10	TEST3/TEST2 = 00 or 11	LED3 = 1	LED2 = X[a]	LED4 = 1

a. X = Don't care

For the 48-pin MLP package, LOM-LED mode and MODE_SEL[1:0] can also be configured using register 1Ch shadow value 01011, bits [4:2] after reset.

Interrupt Function

The B50612D can be programmed to provide an interrupt output based on changes in the PHY status. Each individual interrupt condition is represented by a read-only bit in the "1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah)" on page 111. Interrupts can be individually masked by setting or clearing bits in the interrupt mask register, in "1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh)" on page 114. When an unmasked interrupt condition occurs, programmed LED pins to INTR function are driven low until the interrupt is cleared. Most interrupts are cleared automatically by reading the Interrupt Status register.

The interrupt function can be globally disabled by setting the interrupt disable bit, register 10h, bit 12. The INTR/EnergyDetect pin can be changed to indicate an energy-detect function by setting register 1Ch, shadow value 00100, bit 1= 1.

LED Modes

Many additional LED functions and modes are supported by the B50612D. Table 23 on page 65 describes many of these modes in detail.

The LEDs can be forced on by setting bit 4 of register 10h. This forces all LEDs on continuously. Similarly, the LEDs can be forced off continuously by setting bit 3 of register 10h. This overrides all other LED modes except the force LEDs ON mode. Any LED output pin programmed to be in the INTR mode is open-drain, to allow multiple devices to be connected in a wire-OR fashion. For all other LED modes, LED output pins are continuously driven.

Table 23 on page 65 describes the different modes in which each individual pin can be programmed. For each pin, the modes are listed in order of priority. For example, when the receive LED is programmed to one of the link-utilization modes, the register bit enabling activity/link LED mode is not relevant. The last mode listed for each pin is the default mode.

Multicolor LED

The MULTICOLOR mode uses two programmable LED output pins to control one single LED unit that is capable of producing three different colors: green, amber, red. The multicolor LED mode is enabled by writing value B4AAh to "1000BASE-T/100BASE-TX/10BASE-T LED Selector 1" on page 129. After this register write, the multicolor LED signals appear on LED1 and LED2. Alternatively, the multicolor LED can be output on LED3 and LED4 by writing B8AAh to "1000BASE-T/100BASE-TX/10BASE-T LED Selector 2" on page 131. The subfunction and other parameters can be selected by setting control bits in Table 74 on page 139, "Expansion Register 05h: Multicolor LED Flash Rate Controls" on page 141, and "Expansion Register 06h: Multicolor LED Programmable Blink Controls" on page 142.

Open/Short LED

The OPENSHORT LED is a function of the cable diagnostic mode. The OPENSHORT LED can be programmed to appear on any of the programmable LEDs by writing to the appropriate LED Selector register.

Example: Write value B40Bh to "1000BASE-T/100BASE-TX/10BASE-T LED Selector 1" on page 129.

This LED turns on after the cable diagnostic function is completed and when an open or short is found on any of the four cable pairs attached to the PHY.

Energy Link LED

When one of the programmable LED outputs is programmed in the ENERGYLNK mode, the LED uses blinking and solid on appearances to indicate energy detection and valid links. The ENERGYLNK LED is off when there is no link or energy detected. The LED blinks as soon as energy is detected on the wire. When the link is established, the LED remains continuously on for the duration. Shortly after a loss of energy is detected, the ENERGYLNK LED begins to blink and remains in this state for the length of the Disconnect Timer value, defined in Register 1Ch, Shadow value 10000, bits 3:0. After the timer expires, the LED is turned off.

Additional LED Modes

Some of the LEDs can also be programmed to additional modes. The different modes that each LED output can assume are described in Table 23. Because the modes are listed in the order of priority for each pin, the register bit enabling activity/link LED mode is not relevant when the receive LED is programmed to one of the link utilization modes. The last mode listed for each pin is the default mode. The table is valid for devices configured to RGMII Copper mode only.

Table 23: LED Modes

LEDs	*Description*
All LEDs (except for INTR and OPENSHORT modes)	Force LEDs: • On (register 10h, bit 4 = 1): LED is on solid. • Off (register 10h, bit 3 = 1): LED is off solid.
All LEDs	• General purpose I/O input mode • General purpose I/O output mode (default) Register address 1Ch, shadow value 01111, bits 3:0 = 0000. Each port can be individually programmed to input or output mode.

Table 23: LED Modes (Cont.)

LEDs	*Description*
ACTIVITY LED	Link utilization: This mode provides the estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by 10% increments. For duty cycles of 0.001–10%, the LED blinks at 3 Hz; for duty cycles of 10–20%, the LED blinks at 6 Hz; and for duty cycles of 90–96%, the LED blinks at 30 Hz. Though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. This LED mode is enabled to include all activity, transmit activity only, or receive activity only. • Transmit (register 1Ch, shadow value 01001, bits [1:0] = 01) • Receive (register 1Ch, shadow value 01001, bits [1:0] = 10) • Activity (register 1Ch, shadow value 01001, bits [1:0] = 11) Activity/link LED (register 1Ch, shadow value 01001, bits 4 = 1; register 10h, bit 5 = 0): LED is off when there is no link. The LED is on when there is a link. The LED blinks when the link is up and there is either transmit or receive activity. The LED blinks with a 167 ms cycle and a 50% duty cycle. Receive (register 1Ch, shadow value 01001, bit 3 = 0): This mode expresses receive activity in either of the two modes described below: • Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs. Activity (default): This mode expresses both transmit and receive activity in either of the two modes described below. • Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs.
XMTLED LED	• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for entire cycle if TX activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs.
RCVLED LED	• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if TX activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs.
INTR LED/SD Input (Open Drain)	• Force interrupt (register 10h, bit 11 = 1): LED is forced continuously on. • Disable interrupt (register 10h, bit 12 = 1): LED is forced continuously off. • Normal interrupt (default): LED is forced continuously on until interrupt is cleared.

Table 23: LED Modes (Cont.)

LEDs	*Description*
LOM-LED Mode	In the 48-pin MLP package, if TEST3/TEST2 pins are 00 or 11, LED4 can be used to set the B50612D to enter LOM-LED mode. Active high.

Status	*$\overline{\text{LINKSPD[2]}}$*	*$\overline{\text{LINKSPD[1]}}$*
1000BASE-T	1	0
100BASE-TX	0	1
10BASE-T	1	1
No link	1	1

Note: 0 means LED is turned on.

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Section 4: Register Summary

MII Management Interface Register Programming

The B50612D transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MII management interface registers are written and read serially, using the MDIO and MDC pins. A clock of up to 12.5 MHz must drive the MDC pin of the B50612D. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

Preamble (PRE)

To signal the beginning of an MII instruction after reset, at least 32 consecutive 1 bits must be written to the MDIO pin of the B50612D. A preamble of thirty-two 1 bits is required only for the first read or write following reset. If bit 6 of MII register 01h is cleared, a preamble is always required. A preamble of fewer than thirty-two 1 bits causes the remainder of the instruction to be ignored.

Start of Frame (ST)

A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP)

A read instruction is indicated by 10, while a write instruction is indicated by 01.

PHY Address (PHYAD)

A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.

Register Address (REGAD)

A 5-bit register address follows, with the MSB transmitted first. The addresses for the registers used by the B50612D are shown in Table 25 on page 71.

Turnaround (TA)

The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is performed, 10 must be sent to the B50612D chip during these 2 bit times. When a read operation is performed, the MDIO pin of the MAC must be put in a high-impedance state during these bit times. The B50612D transceiver drives the MDIO pin to 0 during the second bit time.

Data

The last 16 bits of the instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first. During a read operation, the data bits are driven by the B50612D with the MSB transmitted first.

The complete management frame format is summarized in Table 24.

When writing to the MDIO pin, the bit value must be stable for 10 ns before the rising edge of the MDC and must be held valid for 10 ns after the rising edge of the MDC. When reading from the MDIO pin, the data bit is valid at the rising edge of the MDC until the next falling edge of the MDC.

Example: To put a PHY with address 00001 into loopback mode, issue the following write MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000

To determine if a PHY is in the link-pass state, issue the following read MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ

The B50612D drives the MDIO line during the last 17 bit times. If the link status is good, the third bit from the end (bit 2) is 1.

Table 24: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Driven to B50612D Driven by B50612D
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to B50612D

Clause 45 Accesses

Clause 45 accesses are done over the same MDIO/MDC pins as clause 22 accesses. However, the Start of Frame (SF) field is now 00 to signify clause 45. Whereas clause 22 issued the 5-bit address field and the write 16–bit wide write data or read data in the same frame, in clause 45 first an address frame with a 16-bit wide address field is sent to the PHY and is followed by a second frame to perform the read or the write. This allows 65,536 unique addresses to be available in clause 45 register space, whereas clause 22 only allows 32 addresses.

Note: In the B50612D device, Clause 45 accesses are done using Clause 22 per Clause 22.2.4.3.11 and 22.2.4.3.12.

Preamble

To signal the beginning of an MII instruction after reset, at least 32 consecutive 1 bits must be written to the MDIO pin of the B50612D. A preamble (PRE) of thirty-two 1 bits is required only for the first read or write following reset. If bit 6 of MII register 01h is cleared, a preamble is always required. A preamble of fewer than 32 1 bits causes the remainder of the instruction to be ignored.

Start of Frame

A 00 pattern indicates the start of the instruction follows for clause 45 instructions

Operation Code

For Clause 45, an address instruction is indicated by 00, while a write instruction is indicated by 01. A read instruction is indicated by 11, and a read instruction with a post-read increment address instruction is indicated by 10.

PHY Address

In Clause 45, a 5-bit PHY address (PHYAD) follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.

DEVTYPE

In Clause 45, a 5-bit DEVTYPE field follows. For the B50612D, valid DEVTYPEs are 3 (PCS) and 7(AN, 10/100/1000BASE-T).

Turnaround (TA)

The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent to the B50612D chip during these two bit times. When a read operation is being performed, the MDIO pin of the switch must be placed in a high-impedance state during these bit times. The B50612D transceiver drives the MDIO pin to 0 during the second bit time.

Data/Address

In clause 45, the last 16 bits of the instruction are the actual payload, which can be either address or data bits. During an address or write operation, these bits are written to the MDIO pin with the Most Significant Bit (MSB) transmitted first. During a read operation, or a read-increment address operation, the data bits are driven by the B50612D with the MSB transmitted first.

Register Map

Table 25 contains the set of registers for the B50612D transceiver.

Table 25: Register Map

Address	*Register Table*
1000BASE-T/100BASE-TX/10BASE-T Registers	
00h	"1000BASE-T/100BASE-TX/10BASE-T MII Control" on page 73
01h	"1000BASE-T/100BASE-TX/10BASE-T MII Status" on page 75
02h–03h	"1000BASE-T/100BASE-TX/10BASE-T PHY Identifier" on page 78
04h	"1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement" on page 79
05h	"1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Link Partner Ability" on page 81
06h	"1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Expansion" on page 83
07h	"1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit" on page 85
08h	"1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page" on page 86
09h	"1000BASE-T Control" on page 87
0Ah	"1000BASE-T Status" on page 88
0Ch–0Eh	Reserved (do not read from or write to a reserved register)
0Fh	"1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status" on page 90
10h	"1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control" on page 91
11h	"1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status" on page 94
12h	"1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter" on page 96
13h	"1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter" on page 97
14h	"1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter" on page 97
15h–16h	Reserved. (Do not read from or write to a reserved register except for accessing the Expansion registers through register 15h.)
17h	"1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access" on page 98
18h	• "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 98 • "10BASE-T" on page 101 • "1000BASE-T/100BASE-TX/10BASE-T Power/MII Control" on page 104 • "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register" on page 105 • "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control" on page 106
19h	"1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary" on page 108
1Ah	"1000BASE-T/100BASE-TX/10BASE-T Interrupt Status" on page 111
1Bh	"1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask" on page 114

Table 25: Register Map (Cont.)

Address	*Register Table*
1Ch	• "1000BASE-T/100BASE-TX/10BASE-T Spare Control 1" on page 117 • "1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control" on page 119 • "1000BASE-T/100BASE-TX/10BASE-T Spare Control 2" on page 119 • "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3" on page 120 • "1000BASE-T/100BASE-TX/10BASE-T LED Status" on page 121 • "1000BASE-T/100BASE-TX/10BASE-T LED Control" on page 123 • "1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down" on page 125 • "External Control 1 Register" on page 126 • "1000BASE-T/100BASE-TX/10BASE-T LED Selector 1" on page 129 • "1000BASE-T/100BASE-TX/10BASE-T LED Selector 2" on page 131 • "1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status" on page 133
1Dh	• "1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed" on page 134 • "1000BASE-T/100BASE-TX/10BASE-T HCD Status" on page 135
1Eh	"1000BASE-T/100BASE-TX/10BASE-T Test Register 1" on page 138
1Fh	Reserved. (Do not read from or write to a reserved register.)
Registers (Enabled by Register 1Ch, Shadow Value 11111, Bit 0 = 1)	
07h–0Eh	Reserved. (Do not read from or write to reserved register.)
Expansion Registers: Read/Write Through Register 15h (Accessed by Writing to Register 17h, Bits [11:0] = 1111 + Expansion Register Number)	
00h	"Expansion Register 00h: Receive/Transmit Packet Counter" on page 139
04h	"Expansion Register 04h: Multicolor LED Selector" on page 139
05h	"Expansion Register 05h: Multicolor LED Flash Rate Controls" on page 141
06h	"Expansion Register 06h: Multicolor LED Programmable Blink Controls" on page 142
Top-Level Expansion Registers: Read/Write Through Register 15h (Accessed by Writing to Register 17h, Bits [11:0] = 1101 + Top-Level Expansion Register Number) 00h "	
34h	"Top-Level Expansion Register 34h: Spare Register 0" on page 143
40h	"Top-Level Expansion Register 40h: 2K Buffer Register 1" on page 143
41h	"Top-Level Expansion Register 41h: 2K Buffer Register 2" on page 144
Clause 45 Device 7 Registers: Read/Write Through Register 0Dh and 0Eh register. See "Clause 45 Registers" on page 145 ***in detail***	
3Ch	"Clause 45 Device 7 Register Address 3Ch: EEE Advertisement Register" on page 146
803Eh	"Clause 45 Device 7 Register Address 803Eh: EEE Resolution Status Register" on page 147

Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or write:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Self-clearing
- CR = Clear on reset

Reserved bits must be written as the default value and ignored when read.

1000BASE-T/100BASE-TX/10BASE-T Registers Descriptions

1000BASE-T/100BASE-TX/10BASE-T MII Control

Table 26: 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Reset	R/W SC	1 = PHY reset 0 = Normal operation	0
14	Internal Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Speed Selection (LSB)	R/W	Bits [6,13]: 1 1 = Reserved 1 0 = 1000 Mbps 0 1 = 100 Mbps 0 0 = 10 Mbps	0
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	1
11	Power Down	R/W	1 = Power down 0 = Normal operation	0
10	Isolate	R/W	1 = Electrically isolate PHY from RGMII 0 = Normal operation	0
9	Restart Auto-negotiation	R/W SC	1 = Restarting auto-negotiation 0 = Auto-negotiation restart complete	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half-duplex	1
7	Collision Test Enable	R/W	1 = Enable the collision test mode 0 = Disable the collision test mode	0
6	Speed Selection (MSB)	R/W	Work in conjunction with bit 13	1

Table 26: 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
5:0	Reserved	R/W	Write as 00h, ignore on read	00h

Reset

To reset the B50612D by software control, a 1 must be written to bit 15 of the MII Control register. This bit clears itself after the reset process is complete and does not need to be cleared using a second MII write. Writes to other MII Control register bits have no effect until the reset process is completed, which requires approximately 2.0 µs. Writing a 0 to this bit has no effect. A 1 is returned when this bit is read during the reset process; otherwise, it returns a 0.

Internal Loopback

The B50612D can be placed into internal loopback mode by setting bit 14 of the MII Control register. Loopback mode can be cleared by writing a 0 to bit 14 of the MII Control register or by resetting the chip. A 1 is returned when this bit is read and the chip is in loopback mode; otherwise, it returns a 0.

Speed Selection (LSB)

When auto-negotiation is disabled, bits 6 and 13 of the MII Control register can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. When both bits are cleared, 10BASE-T operation is selected. Setting both bits is not permitted. When read, these bits return the last value written.

Auto-Negotiation Enable

When bit 12 of the MII Control register is set, the B50612D mode of operation is controlled by auto-negotiation. When this bit is cleared, the B50612D mode of operation is determined by the Manual Speed, Duplex mode, and Master/Slave Configuration bits. A 1 is returned when this bit is read with auto-negotiation enabled; otherwise, it returns a 0.

Power-Down

When bit 11 of the MII Control register is set, the B50612D is placed into low-power standby mode.

Isolate

The B50612D can be isolated from the RGMII bus by setting bit 10 of the MII Control register. All RGMII outputs are tristated, and all RGMII inputs are ignored. Because the management interface is still active, isolate mode can be cleared by writing a 0 to bit 10 of the MII Control register or by resetting the chip. A 1 is returned when this bit is read and the chip is in isolate mode; otherwise, it returns a 0. The default of this bit is a 0.

Restart Auto-Negotiation

Setting bit 9 of the MII Control register forces the auto-negotiation process to be restarted, regardless of the current state of the auto-negotiation state machine. When auto-negotiation is enabled, setting this bit restarts the auto-negotiation process. Clearing this bit has no effect. This bit is self-clearing. After the auto-negotiation process has restarted, it returns a value of 0.

Duplex Mode

When auto-negotiation is disabled, duplex mode can be controlled by writing to bit 8 of the MII Control register. Setting this bit forces the B50612D into full-duplex operation, and clearing this bit forces the B50612D into half-duplex operation. When this bit is read, it returns the last value written.

Speed Selection (MSB)

When auto-negotiation is disabled, bits 6 and 13 of the MII Control register can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. When both bits are cleared, 10BASE-T operation is selected. Setting both bits is not permitted. When read, these bits return the last value written.

Collision Test

The B50612D can be placed into collision test mode by setting to bit 7 of the MII Control register. In this mode, COL is asserted whenever TX_EN is driven high. The collision test mode can be cleared by writing a 0 to bit 7 of the MII Control register or by resetting the chip. A 1 is returned when this bit is read and the chip is in collision test mode; otherwise, it returns a 0.

1000BASE-T/100BASE-TX/10BASE-T MII Status

Table 27: 1000BASE-T/100BASE-TX/10BASE-T MII Status Register (Address 01h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	100BASE-T4 Capable	RO L	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
14	100BASE-TX Full-duplex Capable	RO H	1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	1
13	100BASE-TX Half-duplex Capable	RO H	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	1
12	10BASE-T Full-duplex Capable	RO H	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1
11	10BASE-T Half-duplex Capable	RO H	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1
10	100BASE-T2 Full-duplex Capable	RO L	1 = 100BASE-T2 full-duplex capable 0 = Not 100BASE-T2 full-duplex capable	0

Table 27: 1000BASE-T/100BASE-TX/10BASE-T MII Status Register (Address 01h) (Cont.)

Bit	Name	R/W	Description	Default
9	100BASE-T2 Half-duplex Capable	RO L	1 = 100BASE-T2 half-duplex capable 0 = Not 100BASE-T2 half-duplex capable	0
8	Extended Status	RO H	1 = Extended status information in reg 0Fh 0 = No extended status information in reg 0Fh	1
7	Reserved	RO	Ignore on read	0
6	Management Frames Preamble Suppression	RO H	1 = Preamble can be suppressed 0 = Preamble always required	1
5	Auto-negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
4	Remote Fault	RO LH	1 = Remote fault detected 0 = No remote fault detected	0
3	Auto-negotiation Ability	RO H	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (link-pass state) 0 = Link is down (link-fail state)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO H	1 = Extended register capabilities 0 = No extended register capabilities	1

100BASE-T4 Capable

The B50612D is not capable of 100BASE-T4 operation and returns a 0 when bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-TX Full-Duplex Capable

The B50612D is capable of 100BASE-TX full-duplex operation and returns a 1 when bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-TX Half-Duplex Capable

The B50612D is capable of 100BASE-TX half-duplex operation and returns a 1 when bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

10BASE-T Full-Duplex Capable

The B50612D is capable of 10BASE-T full-duplex operation and returns a 1 when bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

10BASE-T Half-Duplex Capable

The B50612D is capable of 10BASE-T half-duplex operation and returns a 1 when bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-T2 Full-Duplex Capable

The B50612D is not capable of 100BASE-T2 full-duplex operation and returns a 0 when bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-T2 Half-Duplex Capable

The B50612D is not capable of 100BASE-T2 half-duplex operation and returns a 0 when bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Extended Status

The B50612D contains IEEE Extended Status register at address 0Fh and returns a 1 when bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Management Frames Preamble Suppression

The B50612D accepts MII management frames whether or not they are preceded by the preamble pattern, and returns a 1 when bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Note: Preamble is still required on the first read or write.

Auto-Negotiation Complete

The B50612D returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when auto-negotiation is complete and the contents of registers 4, 5, and 6 are valid. This bit returns a 0 while auto-negotiation is in progress.

Remote Fault

The B50612D returns a 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when its link partner has signaled a remote fault condition. When a remote fault occurs, the bit is set and remains so until the remote fault condition has been cleared and the register is read.

Auto-Negotiation Ability

Even if the auto-negotiation function has been disabled, the B50612D is capable of performing IEEE auto-negotiation and returns a 1 when bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Link Status

The B50612D returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when the link monitor is in the link-pass state (indicating that a valid link has been established); otherwise, it returns a 0. When a link failure occurs, the Link Status bit is latched at 0 and remains so until the bit is read and the B50612D is in the link-pass state.

Jabber Detect

Jabber detection is performed within the PHY and the result is latched into this bit. When a jabber condition has been detected, the B50612D returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register. The bit is cleared by reading.

Extended Capability

The B50612D supports Extended Capability registers and returns a 1 when bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

1000BASE-T/100BASE-TX/10BASE-T PHY Identifier

Table 28: 1000BASE-T/100BASE-TX/10BASE-T PHY Identifier Register (Addresses 02h and 03h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:0	Address 02: ID MSBs	RO	16 MSBs of PHY Identifier	0362h
15:0	Address 03: ID LSBs	RO	16 LSBs of PHY Identifier	5E62h

Note: In the 48-pin MLP package, the register 03h is 5E62h for revision B1.

The IEEE has issued an Organizationally Unique Identifier (OUI) to Broadcom Corporation. This 24-bit number allows devices made by Broadcom to be distinguished from all other manufacturers. The OUI combined with model numbers and revision numbers assigned by Broadcom precisely identifies a device manufactured by Broadcom.

The [15:0] bits of MII register 02h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 03h (PHYID LOW) contain the most significant OUI bits [19:24], 6 Manufacturer's Model Number bits, and 4 Revision Number bits. The two least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-1B-E9, expressed as a hexadecimal value. The binary OUI is 0000-0000-1101-1000-1001-0111. The model number for the B50612D is 26h (100110 binary). Revision numbers start with 1h and are incremented by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + Model[5:0] + Revision [3:0]

Table 28 on page 78 shows the result of concatenating these values to form the PHY identifiers for the B50612D.

1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement

Table 29: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Advertisement Register (Address 04h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Next page ability supported 0 = Next page ability not supported	0
14	Reserved	R/W	Write as 0, ignore on read	0
13	Remote Fault	R/W	1 = Advertise remote fault detected 0 = Advertise no remote fault detected	0
12	Reserved Technology	R/W	Write as 0, ignore on read	0
11	Asymmetric Pause	R/W	1 = Advertise asymmetric pause 0 = Advertise no asymmetric pause	0
10	Pause Capable	R/W	1 = Capable of full-duplex pause operation 0 = Not capable of pause operation	0
9	100BASE-T4 Capable	R/W	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
8	100BASE-TX Full-duplex Capable	R/W	1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	1
7	100BASE-TX Half-duplex Capable	R/W	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	1
6	10BASE-T Full-duplex Capable	R/W	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1
5	10BASE-T Half-duplex Capable	R/W	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1
4:0	Selector Field	R/W	00001 indicates IEEE 802.3 CSMA/CD	00001

Next Page

Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register must be set when the management software wants to control Next Page exchange. When this bit is cleared, Next Page exchange is controlled automatically by the B50612D. When this bit is cleared and the B50612D is not advertising 1000BASE-T capability, no Next Page exchange occurs.

Remote Fault

Setting bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register sends a remote fault indication to the link partner during auto-negotiation. Writing a 0 to this bit clears the Remote Fault transmission bit. This bit returns a 1 when advertising remote fault; otherwise, it returns a 0.

Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is reserved for future versions of the auto-negotiation standard and must always be written as 0.

Asymmetric Pause

When bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50612D advertises that asymmetric pause is preferred. When the bit is cleared, the B50612D advertises that asymmetric pause is not needed. This bit returns a 1 when advertising asymmetric pause; otherwise, it returns a 0. When advertising asymmetric pause, bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register indicates the preferred direction of the pause operation. Setting bit 10 indicates that the pause frames flow toward the B50612D. Clearing bit 10 indicates that pause frames flow toward the link partner.

Pause Capable

When bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50612D advertises full-duplex pause capability. When the bit is cleared, the B50612D advertises no pause capability. This bit returns a 1, when advertising pause capability; otherwise, it returns a 0.

100BASE-T4 Capable

The B50612D does not support 100BASE-T4 capability. Do not write a 1 to bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register.

100BASE-TX Full-Duplex Capable

When bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50612D advertises 100BASE-TX full-duplex capability. When the bit is cleared, the B50612D advertises no 100BASE-TX full-duplex capability. This bit returns a 1 when advertising 100BASE-TX full-duplex capability; otherwise, it returns a 0.

100BASE-TX Half-Duplex Capable

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50612D advertises 100BASE-TX half-duplex capability. When the bit is cleared, the B50612D advertises no 100BASE-TX half-duplex capability. This bit returns a 1 when advertising 100BASE-TX half-duplex capability; otherwise, it returns a 0.

10BASE-T Full-Duplex Capable

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50612D advertises 10BASE-T full-duplex capability. When the bit is cleared, the B50612D advertises no 10BASE-T full-duplex capability. This bit returns a 1 when advertising 10BASE-T full-duplex capability; otherwise, it returns a 0.

10BASE-T Half-Duplex Capable

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register is set, the B50612D advertises 10BASE-T half-duplex capability. When the bit is cleared, the B50612D advertises no 10BASE-T half-duplex capability. This bit returns a 1 when advertising 10BASE-T half-duplex capability; otherwise, it returns a 0.

Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation advertisement register indicate the protocol type. Value 00001 indicates that the B50612D belongs to the 802.3 class of PHY transceivers.

1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Link Partner Ability

Table 30: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Link Partner Ability Register (Address 05h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	RO	1 = Link partner has Next Page ability 0 = Link partner does not have Next Page ability	0
14	Acknowledge	RO	1 = Link partner has received link code word 0 = Link partner has not received link code word	0
13	Remote Fault	RO	1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault	0
12	Reserved Technology	RO	Write as 0, ignore on read	0
11	Asymmetric Pause	RO	1 = Link partner wants asymmetric pause 0 = Link partner does not want asymmetric pause	0
10	Pause Capable	RO	1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation	0
9	100BASE-T4 Capable	RO	1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable	0
8	100BASE-TX Full-duplex Capable	RO	1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable	0

Table 30: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Link Partner Ability Register (Address 05h) (Cont.)

Bit	Name	R/W	Description	Default
7	100BASE-TX Half-duplex Capable	RO	1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner not 100BASE-TX half-duplex capable	0
6	10BASE-T Full-duplex Capable	RO	1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable	0
5	10BASE-T Half-duplex Capable	RO	1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable	0
4:0	Protocol Selector Field	RO	Link partner protocol selector field	00000

Note: As indicated by bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T MII status register, the values contained in the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation link partner ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

Next Page

The B50612D returns a 1 in bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner wants to transmit Next Page information.

Acknowledge

The B50612D returns a 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has acknowledged reception of the link code word; otherwise, it returns a 0.

Remote Fault

The B50612D returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised detection of a remote fault; otherwise, it returns a 0.

Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register is reserved for future versions of the auto-negotiation standard and must be ignored when read.

Asymmetric Pause

The B50612D returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised asymmetric pause; otherwise, it returns a 0.

Pause Capable

The B50612D returns a 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised Pause Capability; otherwise, it returns a 0.

100BASE-T4 Capable

The B50612D returns a 1 in bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-T4 capability; otherwise, it returns a 0.

100BASE-TX Full-Duplex Capable

The B50612D returns a 1 in bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-TX full-duplex capability; otherwise, it returns a 0.

100BASE-TX Half-Duplex Capable

The B50612D returns a 1 in bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-TX half-duplex capability; otherwise, it returns a 0.

10BASE-T Full-Duplex Capable

The B50612D returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 10BASE-T full-duplex capability; otherwise, it returns a 0.

10BASE-T Half-Duplex Capable

The B50612D returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 10BASE-T half-duplex capability; otherwise, it returns a 0.

Protocol Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register return the value of the link partner's advertised Protocol Selector field.

1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Expansion

Table 31: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Expansion Register (Address 06h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	RO	Write as 000h. Ignore on read	003h
4	Parallel Detection Fault	RO LH	1 = Parallel link fault detected 0 = Parallel link fault not detected	0
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability 0 = Link partner does not have Next Page capability	0

Table 31: 1000BASE-T/100BASE-TX/10BASE-T Auto-Negotiation Expansion Register (Address 06h) (Cont.)

Bit	Name	R/W	Description	Default
2	Next Page Capable	RO LH	1 = B50612D is Next Page capable 0 = B50612D is not Next Page capable	1
1	Page Received	RO LH	1 = New page has been received from link partner 0 = New page has not been received	0
0	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation	0

Parallel Detection Fault

When a parallel detection fault has occurred in the auto-negotiation state machine, bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register returns a 1. When a parallel detection fault occurs, this bit is latched at 1 and remains so until the register is read. If a parallel detection fault has not occurred since the last time it was read, this bit returns a 0.

Link Partner Next Page Ability

The B50612D returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register when the link partner needs to transmit Next Page information; otherwise, it returns a 0. This bit is a copy of bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register.

Next Page Capable

When bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register is read, the B50612D supports Next Page capability and returns a 1.

Page Received

The B50612D returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns a 0.

Link Partner Auto-Negotiation Ability

When the link partner shows auto-negotiation capability, the B50612D returns a 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T auto-negotiation expansion register. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns a 0.

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1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit

Table 32: 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit Register (Address 07h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Additional next pages follow 0 = Sending last Next Page	0
14	Reserved	RO	Write as 0, ignore on read	0
13	Message Page	R/W	1 = Formatted page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Complies with message 0 = Cannot comply with message	0
11	Toggle	RO	Toggles between exchanges of different next pages	0
10:0	Message/Unformatted Code Field	R/W	Next page message code or unformatted data	001h

Next Page

Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit register must be set to indicate that more Next Pages are to be sent. This bit must be cleared to indicate that this is the last Next Page to be transmitted. When this bit is read, it returns the last value written.

Message Page

Bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit register must be set to indicate that a formatted message page is being sent. This bit must be cleared to indicate that an unformatted page is being sent. When this bit is read, it returns the last value written.

Acknowledge2

When this bit is set, the B50612D indicates that it can comply with the Next Page request. When this bit is cleared, the B50612D indicates that it cannot comply with the Next Page request. When this bit is read, it returns the last value written.

Toggle

This bit toggles between different Next Page exchanges to ensure a functional synchronization to the link partner.

Message/Unformatted Code Field

These 11 bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when sending formatted pages. When sending unformatted Next Pages, these 11 bits contain an arbitrary data value.

1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page

Table 33: 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page Register (Address 08h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional next pages follow 0 = Sending last Next Page	0
14	Acknowledge	RO	1 = Acknowledge 0 = No acknowledge	0
13	Message Page	RO	1 = Formatted page 0 = Unformatted page	0
12	Acknowledge2	RO	1 = Complies with message 0 = Cannot comply with message	0
11	Toggle	RO	Toggles between exchanges of different next pages	0
10:0	Message Code field	RO	Next Page message code or unformatted data	000h

Next Page

When the link partner has indicated that more Next Pages are to be sent, bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns a 1. This bit returns a 0 when the link partner indicates that this is the last Next Page to be transmitted.

Acknowledge

Bit 14 returns a 1 to indicate that the link partner has received and acknowledged a Next Page. The bit returns a 0 until the link partner has acknowledged the page.

Message Page

Bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns a 1 to indicate that the link partner has sent a formatted message page. This bit returns a 0 when the link partner has sent an unformatted page**.**

Acknowledge2

When the link partner has indicated that it can comply with the Next Page request, bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns a 1. When the link partner has indicated that it cannot comply with the Next Page request, this bit returns a 0.

Toggle

To ensure a functional synchronization to the B50612D transceiver, the link partner toggles this bit between different Next Page exchanges.

Message Code Field

These 11 bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when the link partner has sent a formatted page. When the link partner has sent unformatted next pages, these 11 bits contain an arbitrary data value.

1000BASE-T Control

Table 34: 1000BASE-T Control Register (Address 09h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:13	Test Mode	R/W	1 X X = Test mode 4—Transmitter distortion test 0 1 1 = Test mode 3—Slave transmit jitter test 0 1 0 = Test mode 2—Master transmit jitter test 0 0 1 = Test mode 1—Transmit waveform test 0 0 0 = Normal operation	000
12	Master/Slave Configuration Enable	R/W	1 = Enable master/slave manual configuration value 0 = Automatic master/slave configuration	0
11	Master/Slave Configuration Value	R/W	1 = Configure PHY as master 0 = Configure PHY as slave	0
10	Repeater/DTE	R/W	1 = Repeater/switch device port 0 = DTE device	0
9	Advertise 1000BASE-T Full-duplex Capability	R/W	1 = Advertise 1000BASE-T full-duplex capability 0 = Advertise no 1000BASE-T full-duplex capability	1
8	Advertise 1000BASE-T Half-duplex Capability	R/W	1 = Advertise 1000BASE-T half-duplex capability 0 = Advertise no 1000BASE-T half-duplex capability	0
7:0	Reserved	RO	Write as 0, ignore on read	00h

Test Mode

The B50612D can be placed in one-of-four transmit test modes by writing bits [15:13] of the 1000BASE-T Control register. The transmit test modes are defined in IEEE 802.3ab. When read, these bits return the last value written.

Master/Slave Configuration Enable

When bit 12 of the 1000BASE-T Control register is set, the B50612D master/slave mode is configured using the manual master/slave configuration value. When the bit is cleared, master/slave mode is configured using the automatic resolution function. This bit returns a 1 when manual master/slave configuration is enabled; otherwise, it returns a 0.

Master/Slave Configuration Value

When bit 12 of the 1000BASE-T Control register is set, bit 11 of the 1000BASE-T Control register determines the B50612D master/slave mode of operation. When bit 11 is set, the B50612D is configured as the master. When bit 11 is cleared, the B50612D is configured as the slave. When read, this bit returns the last value written.

Repeater/DTE

When bit 10 of the 1000BASE-T Control register is set, the B50612D advertises that it is a repeater or switch device port. When the bit is cleared, the B50612D advertises that it is a data terminal equipment (DTE) port. The advertised value is used in the automatic master/slave configuration resolution. The link partner, which advertises repeater mode is configured to master if the opposing link partner advertises DTE; otherwise, this bit has no effect. This bit returns a 1 when advertising repeater/switch mode; otherwise, it returns a 0.

Advertise 1000BASE-T Full-Duplex Capability

When bit 9 of the 1000BASE-T Control register is set, the B50612D advertises 1000BASE-T full-duplex capability. When the bit is cleared, the B50612D advertises no 1000BASE-T full-duplex capability. This bit returns a 1 when advertising 1000BASE-T full-duplex capability; otherwise, it returns a 0.

Advertise 1000BASE-T Half-Duplex Capability

When bit 8 of the 1000BASE-T Control register is set, the B50612D advertises 1000BASE-T half-duplex capability. When the bit is cleared, the B50612D advertises no 1000BASE-T half-duplex capability. This bit returns a 1 when advertising 1000BASE-T half-duplex capability; otherwise, it returns a 0.

1000BASE-T Status

Table 35: 1000BASE-T Status Register (Address 0Ah)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Master/Slave Configuration Fault	RO LH	1 = Master/slave configuration fault detected 0 = No master/slave configuration fault detected	0
14	Master/Slave Configuration Resolution	RO	1 = Local transmitter is master 0 = Local transmitter is slave	0
13	Local Receiver Status	RO	1 = Local receiver OK 0 = Local receiver not OK	0
12	Remote Receiver Status	RO	1 = Remote receiver OK 0 = Remote receiver not OK	0
11	Link Partner 1000BASE-T Full-duplex Capability	RO	1 = Link partner is 1000BASE-T full-duplex capable 0 = Link partner not 1000BASE-T full-duplex capable	0

Table 35: 1000BASE-T Status Register (Address 0Ah) (Cont.)

Bit	Name	R/W	Description	Default
10	Link Partner 1000BASE-T Half-duplex Capability	RO	1 = Link partner is 1000BASE-T half-duplex capable 0 = Link partner not 1000BASE-T half-duplex capable	0
9:8	Reserved	RO	Write as 00, ignore on read	00
7:0	Idle Error Count	RO CR	Number of idle errors since last read	00h

Note: As indicated by bit 5 of the MII Status register, the values contained in bits 14, 11, and 10 of the 1000BASE-T Status register are guaranteed to be valid only after auto-negotiation has successfully completed.

Master/Slave Configuration Fault

When a master/slave configuration fault has occurred during auto-negotiation, the B50612D returns a 1 in bit 15 of the 1000BASE-T Status register. When a configuration fault occurs, the bit is latched at 1 and remains so until either the register is read, auto-negotiation is restarted by writing bit 9 in the MII Control register, or auto-negotiation completes successfully with no master/slave configuration fault.

Master/Slave Configuration Resolution

When the B50612D transceiver has been configured as the master, it returns a 1 in bit 14 of the 1000BASE-T Status register. When the B50612D transceiver has been configured as the slave, it returns a 0.

Local Receiver Status

The B50612D transceiver returns a 1 in bit 13 of the 1000BASE-T Status register when the local receiver status is OK; otherwise, it returns a 0.

Remote Receiver Status

The B50612D returns a 1 in bit 12 of the 1000BASE-T Status register when the remote receiver status is OK; otherwise, it returns a 0.

1000BASE-T Full-Duplex Capability

The B50612D returns a 1 in bit 11 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T full-duplex capability; otherwise, it returns a 0.

1000BASE-T Half-Duplex Capability

The B50612D returns a 1 in bit 10 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T half-duplex capability; otherwise, it returns a 0.

Idle Error Count

The B50612D counts the number of idle errors received while the local receiver status is OK. Bits 7 through 0 of the 1000BASE-T Status register return the number of idle errors counted since the last register read. The counter freezes at the maximum value (FFh) to prevent overflow.

1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status

Table 36: 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status Register (Address 0Fh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	1000BASE-X Full-duplex Capable	RO L	1 = 1000BASE-X full-duplex capable 0 = Not 1000BASE-X full-duplex capable	0
14	1000BASE-X Half-duplex Capable	RO L	1 = 1000BASE-X half-duplex capable 0 = Not 1000BASE-X half-duplex capable	0
13	1000BASE-T Full-duplex Capable	RO H	1 = 1000BASE-T full-duplex capable 0 = Not 1000BASE-T full-duplex capable	1
12	1000BASE-T Half-duplex Capable	RO H	1 = 1000BASE-T half-duplex capable 0 = Not 1000BASE-T half-duplex capable	1
11:0	Reserved	RO	Write as 000h, ignore on read	000h

1000BASE-X Full-Duplex Capable

The B50612D is not capable of 1000BASE-X full-duplex operation and returns a 0 when bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-X Half-Duplex Capable

The B50612D is not capable of 1000BASE-X half-duplex operation and returns a 0 when bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T Full-Duplex Capable

The B50612D is capable of 1000BASE-T full-duplex operation and returns a 1 when bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T Half-Duplex Capable

The B50612D is capable of 1000BASE-T half-duplex operation and returns a 1 when bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control

Table 37: 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control Register (Address 10h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as zero	0
14	Disable Automatic MDI Crossover	R/W	1 = Automatic MDI crossover disabled 0 = Automatic MDI crossover enabled	0
13	Transmit Disable	R/W	1 = Transmitter outputs disabled 0 = Normal operation	0
12	Interrupt Disable	R/W	1 = Interrupt status output disabled 0 = Interrupt status output enabled	0
11	Force Interrupt	R/W	1 = Force interrupt status to active 0 = Normal operation	0
10	Bypass 4B/5B Encoder/Decoder (100BASE-TX)	R/W	1 = Transmit and receive 5B codes over MII pins 0 = Normal MII	0
9	Bypass Scrambler/Descrambler (100BASE-TX)	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass MLT3 Encoder/Decoder (100BASE-TX)	R/W	1 = Bypass NRZI/MLT3 encoder and decoder 0 = Normal operation	0
7	Bypass Receive Symbol Alignment (100BASE-TX)	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Reset Scrambler (100BASE-TX)	R/W SC	1 = Reset scrambler to initial state 0 = Normal scrambler operation	0
5	Enable LED Traffic mode	R/W	1 = LED Traffic mode enabled 0 = LED Traffic mode disabled	0
4	Force LEDs On	R/W	1 = Force all LEDs into on state 0 = Normal LED operation	0
3	Force LEDs Off	R/W	1 = Force all LEDs into off state 0 = Normal LED operation	0
2:1	Reserved	R/W	Write as 00, ignore on read	00
0	1000BASE-T PCS transmit FIFO Elasticity (copper mode)	R/W‘	1 = High latency 0 = Low latency	0

MAC/PHY Interface Mode

Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register selects the Interface mode between the MAC and the PHY. This bit must be set to 0 for normal operation.

Disable Automatic MDI Crossover

The automatic MDI crossover function can be disabled by setting bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. When the bit is cleared, the B50612D performs the automatic MDI crossover function (see "Automatic MDI Crossover" on page 30 for details).

Transmit Disable

The transmitter can be disabled by setting bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The transmitter outputs (TRD[3:0]±) are forced into a high-impedance state.

Interrupt Disable

When this bit is set, the interrupt pin is forced to its inactive state except when the Force Interrupt bit is set.

Force Interrupt

When this bit is set, the $\overline{\text{INTR}}$ pin is forced to its active state.

Bypass 4B/5B Encoder/Decoder (100BASE-TX)

The 100BASE-TX 4B/5B encoder/decoder can be bypassed by setting bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The transmitter sends 5B codes from the TX_ER and TXD[3:0] pins directly to the scrambler. TX_EN is ignored and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RX_ER and RXD[3:0] pins. CRS is still asserted when a valid frame is received.

Bypass Scrambler/Descrambler (100BASE-TX)

The 100BASE-TX stream cipher function can be disabled by setting bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The stream cipher function can be reenabled by writing a 0 to this bit.

Bypass MLT3 Encoder/Decoder (100BASE-TX)

The 100BASE-TX MLT3 encoder and decoder can be bypassed by setting bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. NRZ data is transmitted and received on the cable. The MLT3 encoder can be reenabled by clearing this bit.

Bypass Receive Symbol Alignment (100BASE-TX)

100BASE-TX receive symbol alignment can be bypassed by setting bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. When used in conjunction with the bypass 4B/5B encoder/decoder bit, unaligned 5B codes are placed directly on the RX_ER and RXD[3:0] pins.

Reset Scrambler (100BASE-TX)

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50612D resets the scrambler to an all 1 state. This bit is self-clearing and always returns 0 when read.

Enable LED Traffic Mode

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50612D enables the LED traffic mode for ACTIVITYLED and XMITLED. When the bit is cleared, the B50612D disables the LED traffic mode.

Force LEDs On

When bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50612D forces all LEDs into the on state. When the bit is cleared, the B50612D resets all LEDs to normal operation.

Force LEDs Off

When bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the B50612D forces all LEDs into the off state. When the bit is cleared, the B50612D resets all LEDs to normal operation.

1000BASE-T PCS Transmit FIFO Elasticity (Copper Mode)

When bit 0 of the PHY Extended Control register is set, the B50612D sets the FIFO elasticity to high latency. In this mode, the B50612D can transmit packets up to 9 kilobytes in length. When this bit is cleared, the FIFO elasticity is set to low latency. In this mode, the B50612D can transmit packets up to 4.5 kilobytes in length. Setting this bit to 1 adds 16 ns to the 1000BASE-T transmit latency.

1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status

Table 38: 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status Register (Address 11h)

Bit	Name	R/W	Description	Default
15	Auto-Negotiation Base Page Selector Field Mismatch	RO LH	1 = Link Partner Base Page Selector field mismatched Advertised Selector field since last read 0 = No mismatch detected since last read	0
14	Reserved	RO	Write as 0, ignore on read.	0
13	MDI Crossover State	RO	1 = Crossover MDI mode 0 = Normal MDI mode	0
12	Interrupt Status	RO	1 = Unmasked interrupt currently active 0 = Interrupt cleared	0
11	Remote Receiver Status	RO LL	1 = Remote receiver OK 0 = Remote receiver not OK since last read	0
10	Local Receiver Status	RO LL	1 = Local receiver OK 0 = Local receiver not OK since last read	0
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Link Status	RO	1 = Link pass 0 = Link fail	0
7	CRC Error Detected	RO LL	1 = CRC error detected 0 = No CRC error since last read	0
6	Carrier Extension Error Detected	RO LH	1 = Carrier extension error detected since last read 0 = No carrier extension error since last read	0
5	Bad SSD Detected (False Carrier)	RO LH	1 = Bad SSD error detected since last read 0 = No bad SSD error since last read	0
4	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read 0 = No bad ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Auto-Negotiation Base Page Selector Field Mismatch

When this bit is set, the auto-negotiation base page selector does not match the Advertised Selector field since the previous read. When this bit reads back a 0, there is no mismatched Page Selector field and Advertised Selector field.

MDI Crossover State

When the B50612D is automatically switching the transmit and receive pairs to communicate with a remote device, the B50612D returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. This bit returns a 0 when the B50612D is in normal MDI mode.

Interrupt Status

The B50612D returns a 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when any unmasked interrupt is currently active; otherwise, it returns a 0.

Remote Receiver Status

When the remote receiver status is OK, the B50612D returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. When the B50612D detects that the remote receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

Local Receiver Status

When the local receiver status is OK, the B50612D returns a 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. When the B50612D detects that the local receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

Locked

The B50612D returns a 1 in bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when the descrambler is locked to the incoming data stream; otherwise, it returns a 0.

Link Status

The B50612D returns a 1 in bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when the device has established a link; otherwise, it returns a 0.

CRC Error Detected

The B50612D **retur**ns a 1 in bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a CRC error has been detected since the last time this register was read; otherwise, it returns a 0.

Carrier Extension Error Detected

The B50612D returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a carrier extension error has been detected since the last time this register was read; otherwise, it returns a 0.

Bad SSD Detected (False Carrier)

The B50612D returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a bad start-of-stream error has been detected since the last time this register was read; otherwise, it returns a 0.

Bad ESD Detected (Premature End)

The B50612D returns a 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a bad end-of-stream error has been detected since the last time this register was read; otherwise, it returns a 0.

Receive Error Detected

The B50612D returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a packet was received with an invalid code since the last time this register was read; otherwise, it returns a 0.

Transmit Error Detected

The B50612D returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a packet was received with a transmit error code since the last time this register was read; otherwise, it returns a 0.

Lock Error Detected

The B50612D returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if the descrambler has lost lock since the last time this register was read; otherwise, it returns a 0.

MLT3 Code Error Detected

The B50612D returns a 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if an MLT3 coding error has been detected in the receive data stream since the last time this register was read; otherwise, it returns a 0.

1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter

Table 39: 1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter Register (Address 12h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:0	Receive Error Counter	R/W CR	Number of noncollision packets with receive errors since last read	0000h

Receive Error Counter

This counter increments each time the B50612D receives a noncollision packet containing at least 1 receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter

Table 40: 1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter Register (Address 13h)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	Write as 00h, ignore on read	00h
7:0	False Carrier Sense Counter	R/W CR	Number of false carrier sense events since last read	00h

False Carrier Sense Counter

The False Carrier Sense Counter increments each time the B50612D detects a false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter

Table 41: 1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter Register (Address 14h)

Bit	Name	R/W	Description	Default
15:8	Local Receiver NOT_OK Counter	R/W CR	Number of times local receiver was NOT_OK since last read	00h
7:0	Remote Receiver NOT_OK Counter	R/W CR	Number of times B50612D detected that the remote receiver was NOT_OK since last read	00h

Local Receiver NOT_OK Counter

This counter increments each time the local receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Remote Receiver NOT_OK Counter

This counter increments each time the remote receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Note: Receiver NOT_OK Counters (register 14h) becomes 16–bit CRC error counter (CRC errors are counted only after Test Register 1 (Address 1Eh) bit 15 is set to 1).

BROADCOM CONFIDENTIAL
8/17/2016 RCXT3

1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access

Table 42: 1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as 0h, ignore on read	0h
11:8	Expansion Register Select	R/W	1111 = Expansion register selected 0000 = Expansion register not selected All Others= Reserved (Do not use)	0h
7:0	Expansion Register Accessed	R/W	Sets the Expansion register number accessed when read/write to register 15h.	00h

Expansion Register Select

Setting bits [11:8] to 1111 enable the reading from and writing to the Expansion registers through register 15h. These bits should be cleared after the Expansion registers are accessed or when the Expansion registers are not being accessed. See "Expansion Registers" on page 139 for details.

Expansion Register Accessed

Bits [7:0] of the Expansion Register Access register set the Expansion register number accessed. The Expansion register is read/write through register 15h when bits [11:8] of this register are set to 1111. The available expansion registers are listed in the following table.

Table 43: Expansion Register Select Values

Expansion Register	Register Name
00h	"Expansion Register 00h: Receive/Transmit Packet Counter" on page 139
04h	"Expansion Register 04h: Multicolor LED Selector" on page 139
05h	"Expansion Register 05h: Multicolor LED Flash Rate Controls" on page 141
06h	"Expansion Register 06h: Multicolor LED Programmable Blink Controls" on page 142

1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register

Table 44 table lists the available 18h registers.

Table 44: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Values Access

Shadow Value	Register Name
000	"1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 98
001	"10BASE-T" on page 101
010	"1000BASE-T/100BASE-TX/10BASE-T Power/MII Control" on page 104

Table 44: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Values Access (Cont.)

Shadow Value	Register Name
100	"1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register" on page 105
111	"1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control" on page 106

Table 44 shows the read from register 18h, shadow value zzz.

Table 45: Reading Register 18h

Register Reads/Writes	Description
Write register 18h, bits [2:0] = 111	This selects the Miscellaneous Control register, shadow value 111. All reads must be done through the Miscellaneous Control register.
Bit [15] = 0	This allows only bits [14:12] and [2:1] to be written.
Bits [14:12] = zzz	This selects shadow value register zzz to be read.
Bits [11: 3] = <don't care>	When bit [15] = 0, these bits are ignored.
Bits [2:0] = 111	This sets the Shadow Register Select to 111 (Miscellaneous Control register).
Read register 18h	Data read back is the value from shadow register zzz.

Table 46 shows the write to register 18h, shadow value yyy.

Table 46: Writing Register 18h

Register Writes	Description
Set Bits [15:3] = Preferred write values	Bits [15:3] contain the preferred bits to be written to.
Set Bits [2:0] = yyy	This enables shadow value register yyy to be written. For shadow value 111, bit 15 must also be written.

Table 47: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000)

Bit	Name	R/W	Description	Default
15	External Loopback	R/W	1 = External Loopback enabled 0 = Normal operation	0
14	Extended Packet Length	R/W	1 = Allow reception of extended length packets 0 = Allow normal length Ethernet packets only	0
13:11	Reserved	R/W	Write as 0, ignore on read	000
10	Transmit Mode	R/W	1 = Normal operation 0 = Test mode	1
9:8	Reserved	R/W	Write as 0, ignore on read	00

Table 47: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000) (Cont.)

Bit	Name	R/W	Description	Default
7	Disable Partial Response Filter	R/W	1 = Transmitter partial response filter disabled 0 = Transmitter partial response filter enabled	0
6	Reserved	R/W	Write as 0, ignore on read	0
5:4	Edge Rate Control (100BASE-TX)	R/W	00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns	00
3	Reserved	R/W	Write as 0, ignore on read	0
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	000

External Loopback

When bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, external loopback operation is enabled. When the bit is cleared, normal operation resumes.

Extended Packet Length

When bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, the B50612D receives packets up to 18 KB in length. When the bit is cleared, the B50612D only receives packets up to 4.5 KB in length.

Transmit Mode

Bit 10 of the Auxiliary Control register shadow value 000 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register must be set for normal PHY operation.

Disable Partial Response Filter

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, the transmitter partial response filter is disabled. When the bit is cleared, the transmitter partial response filter is enabled.

Edge Rate Control (100BASE-TX)

Bits 5 and 4 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 control the edge rate of the 100BASE-TX transmit DAC output waveform.

Shadow Register Select

The Auxiliary Control register provides access to eight registers using a shadow technique. The lower 3 bits written define which set of 13 upper bits is used in accordance with "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000)" on page 99, defined under bits [2:0]. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 98 describing reading from and writing to register 18h.

The register set previously shown is for normal operation, obtained when the lower 3 bits are 000.

10BASE-T

Table 48: 10BASE-T Register (Address 18h, Shadow Value 001)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Manchester Code Error	RO LH	1 = Manchester code error (10BASE-T) 0 = No Manchester code error	0
14	EOF Error	RO LH	1 = EOF error detected (10BASE-T) 0 = No EOF error detected	0
13	Polarity Error	RO	1 = Channel polarity inverted 0 = Channel polarity correct	0
12	Block RX_DV Extension (IPG)	R/W	1 = Block RX_DV for 4 additional RXC cycles for IPG 0 = Normal operation	0
11	10BASE-T TXC Invert Mode	R/W	1 = Invert TXC output 0 = Normal operation	0
10	Reserved	RO	Write as 0, ignore on read	0
9	Jabber Disable	R/W	1 = Jabber function disabled 0 = Jabber function enabled	0
8:7	Reserved	RO	Write as 0, ignore on read	10
6	10BASE-T Echo Mode	R/W	1 = Echo transmit data to receive data 0 = Normal operation	0
5	SQE Enable Mode	R/W	1 = Enable SQE 0 = Disable SQE	0
4	10BASE-T No Dribble	R/W	1 = Correct 10BASE-T dribble nibble 0 = Normal operation	0
3	Reserved	RO	Write as 0, ignore on read	0

Table 48: 10BASE-T Register (Address 18h, Shadow Value 001) (Cont.)

Bit	Name	R/W	Description	Default
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	001

Manchester Code Error

When a Manchester code violation is received, bit 15 of the 10BASE-T register returns a 1. This bit is valid only during 10BASE-T operation.

EOF Error

When the end-of-frame (EOF) sequence was improperly received (or not received at all), bit 14 of the 10BASE-T register returns a 1. This bit is valid only during 10BASE-T operation.

Polarity Error

When an analog input polarity error has been detected and corrected, bit 13 of the 10BASE-T register returns a 1. This bit is valid only during 10BASE-T operation.

Block RX_DV Extension (IPG)

When bit 12 of the 10BASE-T register is set, blocking of the RX_DV signal is extended for an additional 4 RXC cycles to extend the IPG.

10BASE-T TXC Invert Mode

When bit 11 of the 10BASE-T register is set, the polarity of the 10BASE-T transmit clock is inverted. Clearing this bit restores normal transmit clock polarity. This bit is valid only during 10BASE-T operation.

Jabber Disable

Setting bit 9 of the 10BASE-T register allows the user to disable the jabber detect function defined in the IEEE standard. When a transmission request has exceeded a maximum time limit, this function shuts off the transmitter. Clearing this bit or resetting the chip restores normal operation. Reading this bit returns the value of jabber detect disable. This bit is valid only during 10BASE-T operation.

1000BASE-T Signal Detect Threshold

Setting bit 8 of the 10BASE-T register enables the low 1000BASE-T signal detect threshold. The bit is cleared when in the Normal or Default mode.

10BASE-T Signal Detect Threshold

Setting bit 7 of the 10BASE-T register enables the low 10BASE-T signal detect threshold. The bit is cleared when in the Normal or Default mode.

10BASE-T Echo Mode

When bit 6 of the 10BASE-T register is enabled during 10BASE-T half-duplex transmit operation, the transmitted data is replicated on the receive data pins and the TXEN signal echoes on the RX_DV pin. The TXEN signal also echoes on the CRS pin, and CRS deassertion directly follows the TXEN deassertion.

SQE Enable Mode

Setting bit 5 of the 10BASE-T register enables SQE mode. Clearing disables it. This bit is valid only during 10BASE-T operation.

10BASE-T No Dribble

When bit 4 of the 10BASE-T register is set, the PHY rounds down to the nearest nibble when dribble bits are present on the 10BASE-T input stream.

Shadow Register Select

The 10BASE-T register provides access to 8 registers using shadow technique. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 48 on page 101, defined under bits [2:0]. See the note on “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register” on page 98 describing reading from and writing to register 18h. The register set previously shown is for 10BASE-T operation, obtained when the lower 3 bits are 001.

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1000BASE-T/100BASE-TX/10BASE-T Power/MII Control

Table 49: 1000BASE-T/100BASE-TX/10BASE-T Power/MII Control Register (Address 18h, Shadow Value 010)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as 013h, ignore on read.	013h
5	Super-Isolate	R/W	1 = Isolate mode with no link pulses transmitted 0 = Normal operation	0
4:3	Reserved	R/W	Write as 00, ignore on read	00
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	010

Setting bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Power/MII Control register places the B50612D into the super-isolate mode. Similar to the Isolate mode, all RGMII inputs are ignored and all RGMII outputs are tristated. All link pulses are suppressed.

Shadow Register Select

The 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register provides access to 8 registers using a shadow technique. The lower 3 bits written define which set of 13 upper bit is used in accordance with the table defined under bits [2:0] above. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 98 describing reading from and writing to register 18h.

The register set previously shown is for power/MII control, obtained when the lower 3 bits are 010.

1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register

Table 50: 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test Register (Address 18h, Shadow Value 100)

Bit	Name	R/W	Description	Default
15	Lineside [Remote] Loopback Enable	R/W	1 = Enable lineside [remote] loopback from MDI (cable end) receive packet, through PCS and back to MDI transmit packet. 0 = Disable loopback	0
14:12	Reserved	R/W	Write as 100, ignore on read	100
11	Lineside [Remote] Loopback Tristate	R/W	1 = Tristate the receive MII pins (CRS, RXDV, RXD, and so forth) when lineside [remote] loopback is enabled 0 = Lineside [remote] loopback packets appear on MII	0
10:5	Reserved	R/W	Write as 00h, ignore on read	00h
4	Swap RX MDIX	RO	1 = RX and TX operate on same pair 0 = Normal operation	0
3	10BASE-T Half-Out	R/W	1 = Transmit 10BASE-T at half amplitude 0 = Normal operation	0
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	100

Lineside [Remote] Loopback Enable

Setting bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test register enables lineside (remote) loopback of the copper receive packet back out through the MDI transmit path.

Lineside [Remote] Loopback Tristate

Setting this bit tristates the receive MII pins when the device is in Lineside (remote) Loopback mode.

Swap RX MDIX

When bit 4 of the Miscellaneous Test register is set to a 1, the transmitter and receiver operate on the same twisted pair. This function is for use in a test mode where the transmitter output is detected by the receiver attached to the same pair.

10BASE-T Half-Out

When operating in 10BASE-T mode, setting bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Test register to 1 reduces the output of the transmitter to half of its normal amplitude. Clearing this bit restores full amplitude operation. This function is used in a test mode where an unterminated output generates a signal with twice the amplitude of a terminated output.

Shadow Register Select

The Miscellaneous Test register provides access to 8 registers using a shadow technique. The lower 3 bits written define which set of 13 upper bits is used in accordance with Table 50 under bits [2:0]. See the note on "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 98 describing reading from and writing to register 18h.

The register set previously shown is for miscellaneous testing, obtained when the lower 3 bits are 100.

1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control

Table 51: 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable (Bits 11:3)	R/W SC	1 = Write bits [14:0] 0 = Only write bits [14:12] and [2:0]	0
14:12	Shadow Register Read Selector	R/W	000 = Normal operation 001 = 10BASE-T register 010 = Power Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read.	000
11	Packet Counter Mode	R/W	1 = Receive packet Counter 0 = Transmit Packet Counter	0
10	Reserved	R/W	Write as 0, ignore on read	0
9	Force Auto-MDIX Mode	R/W	1 = Auto-MDIX is enabled when auto-negotiation is disabled 0 = Auto-MDIX is disabled when auto-negotiation is disabled	0
8	RGMII RXD to RXC Skew	R/W	1 = Enable 0 = Disable	1
7:	Reserved	R/W	Write as 0, ignore on read.	

Table 51: 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111) (Cont.)

Bit	Name	R/W	Description	Default
5	RGMII out-of-band status disable	R/W	1 = RXD contains regular RX data during IPG 0 = RXD contains out-of-band status info in RGMII mode during IPG	1
4:3	Reserved	R/W	Write as 0, ignore on read.	00
2:0	Shadow Register Select	R/W	000 = Auxiliary register 001 = 10BASE-T register 010 = Power Control register 011 = Reserved 100 = Miscellaneous Test register 101 = Reserved 110 = Reserved 111 = Miscellaneous Control register	111

Write Enable (Bits 11:3)

If bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register is set when writing to this register, then bits [11:3] of this register can be modified. Bits [2:0] and [14:12] can always be written regardless of the state of bit 15.

When this bit is set, bits [11:3] are written. When this bit is cleared, only bits [14:12] and [2:0] are written.

Shadow Register Read Selector

Bits [14:12] of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register are written, regardless of the value of bit 15. These bits determine the shadow value for an MII register 18h read operation. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 98 describing reading from and writing to register 18h.

Packet Counter Mode

Bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register sets the Packet Counter mode in Expansion register 00h. The counter counts the receive packet when this bit is set; otherwise, it counts the transmit packet.

Force Auto-MDIX Mode

Bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register enable the auto-MDIX mode while auto-negotiation is disabled. The default is to disable the auto-MDIX function when auto-negotiation is disabled.

RXD-to-RXC

Skew time can be increased by approximately 1.9 ns for 1000BASE-T mode, 4 ns for 100BASE-TX mode, and 50 ns for 10BASE-T mode by setting Register 18h, SV 111, bit 8 = 1. Enabling this timing adjustment eliminates the need for board trace delays, as required by the RGMII specification.

RGMII Out-of-Band

In RGMII mode, if this bit is set to 0, RXD contains out-of-band status information during IPG (Inter Packet Gap). If set to 1, RXD contains regular data during IPG.

Shadow Register Select

Using a shadow technique, the 1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control register provides access to 8 registers. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 51, defined under bits 2:0.

See the note on "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page 98 describing reading from and writing to register 18h. The register set previously shown is for miscellaneous control obtained when the lower 3 bits are 111.

1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary

Table 52: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary Register (Address 19h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Auto-negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
14	Auto-negotiation Complete Acknowledge	RO LH	1 = Entered auto-negotiation link good check state 0 = State not entered since last read	0
13	Auto-negotiation Acknowledge Detect	RO LH	1 = Entered auto-negotiation acknowledge detect state 0 = State not entered since last read	0
12	Auto-negotiation Ability Detect	RO LH	1 = Entered auto-negotiation ability detect state 0 = State not entered since last read	1
11	Auto-negotiation Next Page Wait	RO LH	1 = Entered auto-negotiation Next Page wait state 0 = State not entered since last read	0

Table 52: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary Register (Address 19h) (Cont.)

Bit	Name	R/W	Description	Default
10:8	Auto-negotiation HCD (Current Operating Speed and Duplex Mode)	RO	111 = 1000BASE-T full-duplex[a] 110 = 1000BASE-T half-duplex[a] 101 = 100BASE-TX full-duplex[a] 100 = 100BASE-T4 011 = 100BASE-TX half-duplex[a] 010 = 10BASE-T full-duplex[a] 001 = 10BASE-T half-duplex[a] 000 = No highest common denominator or auto-negotiation not complete	000
7	Parallel Detection Fault	RO LH	1 = Parallel link fault detected 0 = Parallel link fault not detected	0
6	Remote Fault	RO	1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault	0
5	Auto-negotiation Page Received	RO LH	1 = New page has been received from link partner 0 = New page has not been received	0
4	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability 0 = Link partner does not perform auto-negotiation	0
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability 0 = Link partner does not have Next Page capability	0
2	Link Status	RO	1 = Link is up (link-pass state) 0 = Link is down (link-fail state)	0
1	Pause Resolution—Receive Direction	RO	1 = Enable pause receive 0 = Disable pause receive	0
0	Pause Resolution—Transmit Direction	RO	1 = Enable pause transmit 0 = Disable pause transmit	0

a. Indicates the negotiated HCD when auto-negotiation enable = 1, or indicates the manually selected speed and Duplex mode when auto-negotiation enable = 0.

Auto-Negotiation Complete

When auto-negotiation is complete, the B50612D returns a 1 in bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register. This bit returns a 0 while auto-negotiation is in progress.

Auto-Negotiation Complete Acknowledge

The B50612D returns a 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the link good check state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation Acknowledge Detect

The B50612D returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the acknowledge detect state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation Ability Detect

The B50612D returns a 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the ability detect state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation Next Page Wait

The B50612D returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the Next Page wait state since the last time this register was read; otherwise, it returns a 0.

Auto-Negotiation HCD (Current Operating Speed and Duplex Mode)

Bits 10:8 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register report the mode of operation negotiated between the B50612D and its link partner. As reported by bit 15 of the Auxiliary Status Summary register, the bits return **000** until auto-negotiation has completed. When the auto-negotiation function has been disabled, bits [10:8] report the manually selected mode of operation.

Parallel Detection Fault

When a parallel detection fault has occurred in the auto-negotiation state machine, bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register returns a 1. When a parallel detection fault occurs, this bit is latched to a 1 and remains so until the next register read. This bit returns a 0 when a parallel detection fault has not occurred since the last time it was read.

Remote Fault

The B50612D returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner has detected a remote fault; otherwise, it returns a 0.

Auto-Negotiation Page Received

The B50612D returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns a 0.

Link Partner Auto-Negotiation Ability

The B50612D returns a 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns a 0.

Link Partner Next Page Ability

The B50612D returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner needs to transmit Next Page information; otherwise, it returns a 0.

Link Status

The B50612D returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link status is good; otherwise, it returns a 0.

Pause Resolution—Receive Direction and Transmit Direction

When auto-negotiation has completed, the B50612D returns the result of the pause resolution function for full-duplex flow control on bits [1:0] of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register. When bit 1 returns a 1, the link partner can send pause frames toward the local device. When bit 0 returns a 1, pause frames can be transmitted by the local device to the link partner. These bits are only guaranteed to be valid when bit 15 of the Auxiliary Status Summary register is 1.

1000BASE-T/100BASE-TX/10BASE-T Interrupt Status

Table 53: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Energy Detect Change	RO LH	1 = Filtered energy detect change since last read (enabled by register 1Ch, shadow 00101, bit 5 = 1) 0 = Interrupt cleared	0
14	Illegal Pair Swap	RO LH	1 = Illegal pair swap detected 0 = Interrupt cleared	0
13	MDIX Status Change	RO LH	1 = MDIX status changed since last read 0 = Interrupt cleared	0
12	Exceeded High Counter Threshold	RO	1 = Value in one or more counters is above 32K 0 = All counters below 32K	0
11	Exceeded Low Counter Threshold	RO	1 = Value in one or more counters is above 128K 0 = All counters below 128K	0
10	Auto-negotiation Page Received	RO LH	1 = Page received since last read 0 = Interrupt cleared	0
9	No HCD Link	RO LH	1 = Negotiated HCD, did not establish link 0 = Interrupt cleared	0

Table 53: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah) (Cont.)

Bit	Name	R/W	Description	Default
8	No HCD	RO LH	1 = Auto-negotiation returned HCD = none 0 = Interrupt cleared	0
7	Negotiated Unsupported HCD	RO LH	1 = Auto-negotiation HCD not supported by B50612D 0 = Interrupt cleared	0
6	Scrambler Synchronization Error	RO LH	1 = Scrambler synchronization error occurred since last read 0 = Interrupt cleared	0
5	Remote Receiver Status Change	RO LH	1 = Remote receiver status changed since last read 0 = Interrupt cleared	0
4	Local Receiver Status Change	RO LH	1 = Local receiver status changed since last read 0 = Interrupt cleared	0
3	Duplex Mode Change	RO LH	1 = Duplex mode changed since last read 0 = Interrupt cleared	0
2	Link Speed Change	RO LH	1 = Link speed changed since last read 0 = Interrupt cleared	0
1	Link Status Change	RO LH	1 = Link status changed since last read 0 = Interrupt cleared	0
0	CRC Error	RO LH	1 = CRC error occurred since last read 0 = Interrupt cleared	0

The $\overline{\text{INTR}}$ output is asserted when any bit in 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register is set and the corresponding bit in the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask register is cleared.

Energy Detect Change

This bit indicates the copper ED changed since the last read.

Illegal Pair Swap

The B50612D returns a 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when an uncorrectable pair swap error on the twisted-pair cable has been detected since the last time this register was read; otherwise, it returns a 0.

MDIX Status Change

The B50612D returns a 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a link pulse or 100BASE-TX carrier was detected on a different pair than previously detected since the last time this register was read; otherwise, it returns a 0.

Exceeded High Counter Threshold

The B50612D returns a 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when one or more of the counters in registers 12–14h is above 32 000; otherwise, it returns a 0.

Exceeded Low Counter Threshold

The B50612D returns a 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when one or more of the counters in registers 12–14h is above 128 000; otherwise, it returns a 0.

Auto-Negotiation Page Received

The B50612D returns a 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns a 0.

No HCD Link

When the negotiated HCD is not able to establish a link, bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns a 1 by the B50612D. The bit is cleared when the register is read.

No HCD

When auto-negotiation returns no HCD, bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns a 1 by the B50612D. The bit is cleared when the register is read.

Negotiated Unsupported HCD

When the auto-negotiation HCD is not supported by the B50612D, bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns a 1. The B50612D does not support 100BASE-T4. The bit is cleared when the register is read.

Scrambler Synchronization Error

The B50612D returns a 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a scrambler synchronization error has been detected since the last time this register was read; otherwise, it returns a 0.

Remote Receiver Status Change

The B50612D returns a 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the remote receiver status has changed since the last time this register was read; otherwise, it returns a 0.

Local Receiver Status Change

The B50612D returns a 1 in bit 4 of the Interrupt Status register when the local receiver status has changed since the last time this register was read; otherwise, it returns a 0.

Duplex Mode Change

The B50612D returns a 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the Duplex mode has changed since the last time this register was read; otherwise, it returns a 0.

Link Speed Change

The B50612D returns a 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the link speed has changed since the last time this register was read; otherwise, it returns a 0.

Link Status Change

The B50612D returns a 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the link status has changed since the last time this register was read; otherwise, it returns a 0.

CRC Error

The B50612D returns a 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a receive CRC error has been detected since the last time this register was read; otherwise, it returns a 0.

1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask

Table 54: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Energy Detect Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
14	Illegal Pair Swap	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
13	MDIX Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
12	Exceeded High Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1

Table 54: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh) (Cont.)

Bit	Name	R/W	Description	Default
11	Exceeded Low Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
10	Auto-negotiation Page Received	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
9	HCD No Link	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
8	No HCD	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
7	Negotiated Unsupported HCD	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
6	Scrambler Synchronization Error	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
5	Remote receiver status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
4	Local receiver status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
3	Duplex mode Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
2	Link Speed Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1
1	Link Status Change	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1

Table 54: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh) (Cont.)

Bit	Name	R/W	Description	Default
0	CRC Error	R/W	1 = Interrupt masked, status bits operate normally. 0 = Interrupt enabled, status bits operate normally.	1

Interrupt Mask Vector

When bit *n* of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask register is written to 1, the interrupt corresponding to the same bit in the Interrupt Status register is masked. The status bits still operate normally when the interrupt is masked, but do not generate an interrupt output. When the bit is written to 0, the interrupt is unmasked.

1000BASE-T/100BASE-TX/10BASE-T Register 1Ch Access

Reading and writing to the 1000BASE-T/100BASE-TX/10BASE-T register 1Ch is through register 1Ch bits 15:10. Bits 14:10 set the shadow value of register 1Ch, and bit 15 enables the writing of the bits 9:0. Setting bit 15 allows writing to bits [9:0] of register 1Ch. To read register 1C shadow zzzzz, set writes to register 1Ch with bit 15 = 0 and bits 14:10 to zzzzz first. The subsequent register read from register 1Ch contains the shadow zzzzz register value. All of the register 1Ch shadow values are listed in the following table.

Table 55: 1000BASE-T/100BASE-TX/10BASE-T Register 1Ch Shadow Values

Shadow Value	Register Name
00010	“1000BASE-T/100BASE-TX/10BASE-T Spare Control 1” on page 117
00011	“1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control” on page 119
00100	“1000BASE-T/100BASE-TX/10BASE-T Spare Control 2” on page 119
00101	“1000BASE-T/100BASE-TX/10BASE-T Spare Control 3” on page 120
01000	“1000BASE-T/100BASE-TX/10BASE-T LED Status” on page 121
01001	“1000BASE-T/100BASE-TX/10BASE-T LED Control” on page 123
01010	“1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down” on page 125
01011	“External Control 1 Register” on page 126
01101	“1000BASE-T/100BASE-TX/10BASE-T LED Selector 1” on page 129
01110	“1000BASE-T/100BASE-TX/10BASE-T LED Selector 2” on page 131
01111	“1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status” on page 133

1000BASE-T/100BASE-TX/10BASE-T Spare Control 1

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register 1Ch with the shadow value in bits [14:10] = 00010.

Table 56: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00010 = Spare Control 1 register	00010
9:4	Reserved	R/W	Write as 00h, ignore when read.	00h
3	Reserved	R/W	Write as 00h, ignore when read.	00h
2	Linkspeed	R/W	0 = Normal 1 = Dual Link speed indication	0
1	Reserved	R/W	Write as 00h, ignore when read.	1
0	Link LED Mode	R/W	1 = Enable link LED mode LINKSPD[2:1] = speed 00: 1000BASE-T link 01: 100BASE-TX link 10: 10BASE-T link or no link SLAVE = Active low 10/100/1000BASE-T link 0 = Normal link LED mode	0

Write Enable

During a write to this register, setting Spare Control 1 register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 00010 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register address 1Ch.

Linkspeed

When Linkspeed bit is 0 (default), LINKSPD[2] and LINKSPD[1] provide link status as shown in Table 57.

Table 57: Default LED1 and LED2 Status

Status	*LINKSPD[2]*	*LINKSPD[1]*
1000BASE-T link	0	0
100BASE-TX link	0	1
10BASE-T link	1	0
No link	1	1

Note: Using this mode, it is possible to connect LED1 and LED2 pins directly to a back-to-back connected, integrated LED block that can indicate a 1000BASE-T link or a 100BASE-TX gigabit link only.

When Linkspeed bit is 1, LINKSPD[2] and LINKSPD[1] provide link status as shown in Table 58.

Table 58: Linkspeed LED1 and LED2 Status (LOM-LED Mode)

Status	*LINKSPD[2]*	*LINKSPD[1]*
1000BASE-T link	1	0
100BASE-TX link	0	1
10BASE-T link	1	1
No link	1	1

Link LED Mode

Bit 0 of 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register 1Ch with shadow value 00010 selects the link LED mode. When this bit is set, it enables the link LED mode. The LINKSPD2/LINKSPD1 are Link/Speed LED and SLAVE LED is LINK LED to indicate a link for 10BASE-T, 100BASE-TX, or 1000BASE-T. When this bit is cleared, the LINKSPD2, LINKSPD1, and SLAVE are in normal mode.

1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control register 1Ch with shadow value in bits [14:10] = 00011.

Table 59: 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control Register (Address 1Ch, Shadow Value 00011)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00011 = Clock Alignment Control register	00011
9	GTXCLK Clock Delay Enable	R/W	1 = Enable GTXCLK delay 0 = Normal mode (bypass GTXCLK delay)	1
8:0	Reserved	R/W	Write as 000h, ignore when read.	000h

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 00011 to enable read/write to the Clock Alignment Control register address 1Ch.

GTXCLK Clock Delay Enable

Setting bit 9 of 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control register 1Ch with shadow value 00011 enables the GTXCLK internal delay. When this bit is cleared, the GTXCLK delay is bypassed.

1000BASE-T/100BASE-TX/10BASE-T Spare Control 2

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 00100.

Table 60: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 Register (Address 1Ch, Shadow Value 00100)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0

Table 60: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 Register (Address 1Ch, Shadow Value 00100) (Cont.)

Bit	Name	R/W	Description	Default
14:10	Shadow Register Selector	R/W	00100 = Spare Control 2 register	00100
9:5	Reserved	R/W	Write as 00h, ignore when read.	00h
4:2	Reserved	R/W	Write as 011, ignore on read.	011
1	Energy Detect on INTR Pin	R/W	1 = Routes Energy Detect to interrupt signal. Use LED selectors (register 1Ch shadow 01101 and 01110) and program to INTR mode. 0 = INTR pin is Interrupt function.	0
0	Reserved	R/W	Write as 0, ignore when read.	0

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] must be set to 00100 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 register.

Energy Detect on INTR Pin

Bit 1 enables the signal detect or energy detect input on the INTR pin. Set the LED selector register to enable INTR LED mode (1Ch shadow 01101 or 01110 set bit [7:4]/[3:0] to 0110 depending on the LED).

1000BASE-T/100BASE-TX/10BASE-T Spare Control 3

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 00101.

Table 61: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00101 = Spare Control 3 register	00101
9	Reserved	R/W	Write as 0, ignore when read.	0

Table 61: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101) (Cont.)

Bit	Name	R/W	Description	Default
8	TXC/RXC Disable During Auto Power-Down	R/W	1 = Disable TXC/RXC during auto power-down when there is not energy on the cable.	0
7:2	Reserved	R/W	Write as 07h, ignore when read.	07
1	DLL Auto Power-Down	R/W	1 = Auto power down of DLL is disabled. 0 = Auto power down of DLL is enabled.	
0	Reserved	–	–	1

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow register values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 00101 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 register.

TXC/RXC Disable During Auto Power-Down Mode

Setting this bit=1, disables the TXC/RXC during auto power-down. This feature enables additional power savings. This feature should only be used during auto power-down mode.

DLL Auto Power-Down

Clearing this bit enables the auto power-down mode of the internal DLL. This feature enables additional power savings. This feature should only be used during auto power-down mode.

1000BASE-T/100BASE-TX/10BASE-T LED Status

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01000.

Table 62: 1000BASE-T/100BASE-TX/10BASE-T LED Status Register (Address 1Ch, Shadow Value 01000)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01000 = LED Status register	01000

Table 62: 1000BASE-T/100BASE-TX/10BASE-T LED Status Register (Address 1Ch, Shadow Value 01000) (Cont.)

Bit	Name	R/W	Description	Default
9	Reserved	R/O	Write as 0, ignore when read.	0
8	$\overline{\text{Slave}}$ Indicator	RO	1 = Master mode 0 = Slave mode	0
7	$\overline{\text{FDX}}$ Indicator	RO	1 = Half-duplex mode 0 = Full-duplex mode	0
6	$\overline{\text{INTR}}$ Indicator	RO	1 = No active Interrupt 0 = Interrupt activated	1
5	Reserved	RO	Write as 0, ignore when read.	0
4:3	$\overline{\text{LINKSPD}}$ Indicator	RO	11 = No link 10 = 10BASE-T LINK 01 = 100BASE-TX LINK 00 = 1000BASE-T LINK	11
2	$\overline{\text{Transmit}}$ Indicator	RO	1 = No transmit activity 0 = Transmit activity	1
1	$\overline{\text{Receive}}$ Indicator	RO	1 = Not receive activity 0 = Receive activity	1
0	Reserved	RO	Write as 0, ignore when read.	1

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01000 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Status register.

$\overline{\text{Slave}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 8 returns a 0, the device is in the slave mode. When this bit returns a 1, the device is not in the slave mode.

$\overline{\text{FDX}}$ Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 7 returns a 0, the device is in the full-duplex mode. When this bit returns a 1, the device is not in the full-duplex mode.

INTR Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 6 returns a 0, the device is in the interrupted mode. When this bit returns a 1, the device is not in the interrupted mode.

LINKSPD Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bits 4:3 return a 00, the device is in the 1000BASE-TX Link mode. When these bits return a 01, the device is in the 100BASE-TX link mode. When these bits return a 10, the device is in the 10BASE-T link mode. When these bits return an 11, the device is not linked.

Transmit Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 2 returns a 0, the device is in transmit mode. When this bit returns a 1, the device is not in transmit mode.

Receive Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 1 returns a 0, the device is in receive mode. When this bit returns a 1, the device is not in receive mode.

1000BASE-T/100BASE-TX/10BASE-T LED Control

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01001.

Table 63: 1000BASE-T/100BASE-TX/10BASE-T LED Control Register (Address 1Ch, Shadow Value 01001)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01001 = LED Control register	01001
9:6	Reserved	R/W	Write as 00000, ignore when read.	00000
5	Reserved	R/W	Write as 0, ignore when read.	0
4	Activity/Link LED Enable	R/W	1 = Drive activity/link data on $\overline{\text{ACTIVITY}}$ LED 0 = Drives activity data on $\overline{\text{ACTIVITY}}$ LED	0
3	$\overline{\text{ACTIVITY}}$ LED Enable	R/W	1 = Drive activity data on $\overline{\text{ACTIVITY}}$ LED 0 = Drive receive data on $\overline{\text{ACTIVITY}}$ LED	1
2	Remote Fault LED Enable	R/W	Indicate remote fault 1 = Indicate remote fault 0 = Normal operation	0

Table 63: 1000BASE-T/100BASE-TX/10BASE-T LED Control Register (Address 1Ch, Shadow Value 01001) (Cont.)

Bit	Name	R/W	Description	Default
1:0	Link Utilization LED Selector	R/W	00 = Normal activity (fixed blink rate) 01 = Transmit activity with variable blink rate 10 = Receive activity with variable blink rate 11 = Transmit/receive activity with variable blink rate ***Note:*** This mode has higher priority than the activity LED Enable mode in bit 3.	00

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01001 to enable read/write to the register address 1Ch.

Activity/Link LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 4 drives activity/link data on $\overline{\text{ACTIVITY}}$ LED.

$\overline{\text{ACTIVITY}}$ LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 3 drives activity data on $\overline{\text{ACTIVITY}}$ LED. Otherwise, it drives receive data on ACTIVITY LED.

Remote Fault LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 2 drives remote fault LED.

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Link Utilization LED Selector

These bits apply to the LED programmed to the ACTIVITY mode only. In the activity LED mode, the LED expresses an estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by increments of 10%. For duty cycles of 0.001% to10%, the LED blinks at 3 Hz; for duty cycles of 10% to 20%, the LED blinks at 6 Hz; and for duty cycles of 90% to 96%, the LED blinks at 30 Hz. Even though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. The ACTIVITY LED can be programmed to display the following:

- 00 = Normal activity (fixed blink rate)
- 01 = Transmit activity with variable blink rate
- 10 = Receive activity with variable blink rate
- 11 = Transmit/receive activity with variable blink rate

1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register 1Ch with shadow value in bits [14:10] = 01010.

Table 64: Auto Power-Down Register (Address 1Ch, Shadow Value 01010)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01010 = Auto Power-Down register	01010
9:6	Reserved	R/W	Write as 0h, ignore when read.	0h
5	Auto Power-Down Mode	R/W	1 = Auto power-down mode enabled 0 = Auto power-down mode disabled	
4	Sleep Timer Select	R/W	1 = Sleep timer is 5.4s. 0 = Sleep timer is 2.7s.	0
3:0	Wake-up Timer Select	R/W	Counter for wake-up timer in units of 84 ms. 0001 = 84 ms 0010 = 168 ms ... 1111 = 1.26s	0001

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 01010 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register address 1Ch.

Auto Power-Down Mode

Setting this bit enables the auto power-down mode.

Sleep Timer Select

Setting this bit changes the wake-up time leaving auto power-down mode.

Wake-up Timer Select

The port continues wake-up mode for a time based on the count stored in this register. The minimum value is 84 ms and the maximum value is 1.26s. This only applies when the part is in auto power-down mode.

External Control 1 Register

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01011.

Table 65: External Control 1 Register (Address 1Ch, Shadow Value 01011)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0], 0 = Read bits [9:0].	0
14:10	Shadow Register Selector	R/W	01011 = External Control 1 register	01011
9:8	Reserved	R/W	Write as 0h, ignore when read.	0h
7	CLK125 Disable	R/W	1 = CLK125 clock output disable 0 = CLK125 clock output enable	0
6	Soft-Reset Enable	R/W	1 = Soft-reset function enable 0 = Soft-reset function disable	0
5	Reserved	R/W	Write as 0h, ignore when read.	0h
4	MODE_SEL[1]	R/W	MODE_SEL[1], in 48-pin MLP package only	LED3 pin
3	MODE_SEL[0]	R/W	MODE_SEL[0], in 48-pin MLP package only	LED2 pin
2	LOM-LED Mode	R/W	1 = LOM-LED mode enabled, in 48-pin MLP package only 0 = LOM-LED mode disabled, in 48-pin MLP package only.	LED4 pin
1: 0	Reserved	R/W	Write as 0h, ignore when read.	0h

Write Enable

During a write to this register, setting External Control 1 register bit 15 to a 1 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 01011 to enable read/write to the External Control 1 register address 1Ch.

CLK125 Disable

In the 48-pin MLP package, this bit is not used.

Soft-Reset Enable

Register bit 6 enables the soft-reset feature. After this feature is enabled, setting PHY register 0x00h bit 15 to 1 invokes a soft reset, which resets everything expect for the MDIO registers.

After enabling the soft-reset function, the PHY register 0x00h bit 15 will not be able to self clear. Write a “0” to bit 15 of the MII Control register (address 00h) to clear it after software reset.

MODE_SEL[1:0]

Setting these bits selects the different RGMII MODE.

LOM-LED Mode

Setting this bit enables LOM-LED MODE.

External Control 2 Register

The following is enabled by External Control 2 Register register 1Ch with shadow value in bits [14:10] = 01100.

Table 66: External Control 2 Register (Address 1Ch, Shadow Value 01100)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01100 = External Control 2 register	01100
9:6	Reserved	R/W	Write as 00, ignore when read.	0h
5	Enable IDDQ-SR	R/W	1 = Enable IDDQ-SR mode. 0 = Normal operation.	0
4	Enable IDDQ-SD	R/W	1 = Enable IDDQ-SD mode. 0 = Normal operation.	0
3:1	Reserved	R/W	Write as 0h, ignore when read.	0h
0	Enable IDDQ-LP	R/W	1 = Enable IDDQ-LP mode. 0 = Normal operation.	0

Write Enable

During a write to this register, setting External Control 2 register bit 15 to a 1 allows writing to bits [7:0] of this register. For reading the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01100 to enable read/write to the External Control 2 register address 1Ch.

Enable IDDQ-SR

The B50612D can be placed into the ultra-low power-down mode with Soft Recovery (IDDQ-SR). This bit must be used with bit 0 (Enable IDDQ) at the same time.

Enable IDDQ-SD

The B50612D can be placed into the ultra-low power-down mode with Signal Detect (IDDQ-SD).

Enable IDDQ-LP

The B50612D can be placed into the ultra-low power-down mode (IDDQ), consuming the lowest power possible while voltage is being supplied to the device. This mode is especially useful for saving battery life in laptop designs when the user does not require a network connection.

1000BASE-T/100BASE-TX/10BASE-T LED Selector 1

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value in bits [14:10] = 01101.

Table 67: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01101 = LED Selector 1 register	01101
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED2 Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{LED2/FDX}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{REMOTE FAULT}}$ 1000: $\overline{\text{RCVLED}}$ 1001: $\overline{\text{Wirespeed downgrade}}$ 1010: $\overline{\text{MULTICOLOR[2]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0001

Table 67: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101) (Cont.)

Bit	Name	R/W	Description	Default
3:0	LED1 Selector	R/W	0000: LINKSPD[1] 0001: LINKSPD[2] 0010: XMITLED 0011: ACTIVITYLED 0100: LED2/FDX 0101: SLAVE 0110: INTR 0111: REMOTE FAULT 1000: RCVLED 1001: Wirespeed downgrade 1010: MULTICOLOR[1] 1011: OPENSHORT 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0000

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Selector register 1 bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01101 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Selector register 1 address 1Ch.

LED2 (LINKSPD[2]) Selector

Bits [7:4] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value 01101 select the LED2 mode.

LED1 (LINKSPD[1]) Selector

Bits [3:0] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value 01101 select the LED1 mode.

1000BASE-T/100BASE-TX/10BASE-T LED Selector 2

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value in bits [14:10] = 01110.

Table 68: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 Register (Address 1Ch, Shadow Value 01110)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01110 = LED Selector 2 register	01101
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED2 Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{LED2/FDX}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{REMOTE FAULT}}$ 1000: RCVLED 1001: Reserved 1010: $\overline{\text{MULTICOLOR[2]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0001
3:0	LED1 Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{LED2/FDX}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{REMOTE FAULT}}$ 1000: RCVLED 1001: Reserved 1010: $\overline{\text{MULTICOLOR[1]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: Reserved 1101: Reserved 1110: Off (high) 1111: On (low)	0000

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Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register bit 15 to a 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to a 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01110 to enable read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register address 1Ch.

LED4 ($\overline{\text{INTR}}$) Selector

Bits [7:4] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value 01110 select the LED2 mode.

LED3 ($\overline{\text{ACTIVITYLED}}$) Selector

Bits [3:0] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value 01110 select the LED1 mode.

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status

The following is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register 1Ch with shadow value in bits [14:10] = 01111.

Table 69: 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status Register (Address 1Ch, Shadow Value 01111)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01111 = LED GPIO Control/Status register	01111
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED I/O Status	RO	Bit 7: LED4 pin status Bit 6: LED3 pin status Bit 5: LED2 pin status Bit 4: LED1 pin status 1 = LED pin is an input. 0 = LED pin is an output.	0h
3:0	Programmable LED I/O Control	R/W	Bit 3: LED4 pin control Bit 2: LED3 pin control Bit 1: LED2 pin control Bit 0: LED1 pin control 1 = Disable LED output 0 = Enable LED output	0h

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [14:10] must be set to 01111 to enable read/write to the register address 1Ch.

LED I/O Status

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [7:4] read back the status of the LED pin.

Programmable LED I/O Control

Setting 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [3:0] sets the LED pin to disable LED output. Clearing LED GPIO Control/Status register bits [3:0] sets the LED pin to enable LED output.

1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed

Table 70: 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed Register (Address 1Dh) Bit 15=0

Bit	*Name*	*R/W*	*Description*	*Default*
15	Enable Shadow Register	R/W	1 = Select shadow register 0 = Normal operation Writes to the selected register are done on a single cycle.	0
14	Master/Slave Seed Match	RO LH	1 = Seeds match. 0 = Seeds do not match.	0
13	Link Partner Repeater/DTE Bit	RO	1 = Link partner is a repeater/switch device port. 0 = Link partner is a DTE device port.	0
12	Link Partner Manual Master/ Slave Configuration Value	RO	1 = Link partner is configured as master. 0 = Link partner is configured as slave.	0
11	Link Partner Manual Master/ Slave Configuration Enable	RO	1 = Link partner manual master/slave configuration enabled 0 = Link partner manual master/slave configuration disabled	0
10:0	Local Master/Slave Seed Value	R/W	Returns the automatically generated M/S random seed.	000h

Enable Shadow Register

When bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register is cleared, the Master/Slave Seed register is selected. If bit 15 is set, the shadow HCD Status register is selected for read/write.

Master/Slave Seed Match

Bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1 when the master/slave seed matches; otherwise, it returns a 0.

Link Partner Repeater/DTE Bit

When this read-only bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1, it indicates that the link partner is configured as a repeater or a switch. If this bit returns a 0, it indicates that the link partner is configured as a DTE port.

Link Partner Manual Master/Slave Configuration Value

When this read-only bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1, it indicates that the link partner is configured as a master. If this bit returns a 0, it indicates that the link partner is configured as a slave.

Link Partner Manual Master/Slave Configuration Enable

When this read-only bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns a 1, it indicates that the link partner manual master/slave configuration is enabled. If this bit returns a 0, the link partner manual master/slave configuration is disabled.

Local Master/Slave Seed Value

Bits [10:0] of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register return the automatically generated local master/slave seed value.

1000BASE-T/100BASE-TX/10BASE-T HCD Status

Table 71: 1000BASE-T/100BASE-TX/10BASE-T HCD Status Register (Address 1Dh) Bit 15=1

Bit	*Name*	*R/W*	*Description*	*Default*
15	Enable Shadow Register	R/W	1 = Select Shadow register 0 = Normal operation	0
14	Reserved	RO	Write as 0, ignore on read	0
13	Reserved	RO	Write as 0, ignore on read	0
12	Reserved	RO LH	Write as 0, ignore on read	0
11	HCD 1000BASE-T FDX	RO LH	1 = Gigabit full-duplex occurred since last read 0 = HCD cleared	0
10	HCD 1000BASE-T	RO LH	1 = Gigabit half-duplex occurred since last read 0 = HCD cleared	0
9	HCD 100BASE-TX FDX	RO LH	1 = 100BASE-TX full-duplex occurred since last read 0 = HCD cleared	0
8	HCD 100BASE-TX	RO LH	1 = 100BASE-TX half-duplex occurred since last read 0 = HCD cleared	0
7	HCD 10BASE-T FDX	RO LH	1 = 10BASE-T full-duplex occurred since last read 0 = HCD Cleared	0
6	HCD 10BASE-T	RO LH	1 = 10BASE-T half-duplex occurred since last read 0 = HCD cleared	0
5	HCD 1000BASE-T FDX (Link Never Came Up)	RO LH	1 = Gigabit full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0

Table 71: 1000BASE-T/100BASE-TX/10BASE-T HCD Status Register (Address 1Dh) Bit 15=1 (Cont.)

Bit	Name	R/W	Description	Default
4	HCD 1000BASE-T (Link Never Came Up)	RO LH	1 = Gigabit half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
3	HCD 100BASE-TX FDX (Link Never Came Up)	RO LH	1 = 100BASE-TX full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
2	HCD 100BASE-TX (Link Never Came Up)	RO LH	1 = 100BASE-TX half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
1	HCD 10BASE-T FDX (Link Never Came Up)	RO LH	1 = 10BASE-T full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
0	HCD 10BASE-T (Link Never Came Up)	RO LH	1 = 10BASE-T half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0

Note: Bits 12:0 are cleared when auto-negotiation is disabled using MII register 0 bit 12 or restarted using MII register 0 bit 9.

Enable Shadow Register

When bit 15 of 1000BASE-T/100BASE-TX/10BASE-T HCD Status register is cleared, the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register is selected. If bit 15 is set, the shadow HCD Status register (auto-negotiation highest common denominator resolution) is selected for read/write. This bit must set to be able to read/write to the HCD Status register.

HCD 1000BASE-T FDX

When bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit full-duplex HCD has occurred since the last read.

HCD 1000BASE-T

When bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit half-duplex HCD has occurred since the last read.

HCD 100BASE-TX FDX

When bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX full-duplex HCD has occurred since the last read.

HCD 100BASE-TX

When bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX half-duplex HCD has occurred since the last read.

HCD 10BASE-T FDX

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T full-duplex HCD has occurred since the last read.

HCD 10BASE-T

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T half-duplex HCD has occurred since the last read.

HCD 1000BASE-T FDX (Link Never Came Up)

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit full-duplex HCD has occurred, but the link has not been established since the last read.

HCD 1000BASE-T (Link Never Came Up)

When bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a Gigabit half-duplex HCD has occurred, but the link has not been established since the last read.

HCD 100BASE-TX FDX (Link Never Came Up)

When bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX full-duplex HCD has occurred, but the link has not been established since the last read.

HCD 100BASE-TX (Link Never Came Up)

When bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 100BASE-TX half-duplex HCD has occurred, but the link has not been established since the last read.

HCD 10BASE-T FDX (Link Never Came Up)

When bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T full-duplex HCD has occurred, but the link has not been established since the last read.

HCD 10BASE-T FDX (Link Never Came Up)

When bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns a 1, it indicates that a 10BASE-T half-duplex HCD has occurred, but the link has not been established since the last read.

1000BASE-T/100BASE-TX/10BASE-T Test Register 1

Table 72: 1000BASE-T/100BASE-TX/10BASE-T Test Register 1 (Address 1Eh)

Bit	Name	R/W	Description	Default
15	CRC Error Counter Selector	R/W	1 = Receiver NOT_OK Counters (register 14h) becomes 16-bit CRC error counter (CRC errors are counted only after this bit is set). 0 = Normal operation	0
14:13	Reserved	R/W	Write as 00h, ignore when read.	00
12	Force Link 10/100/ 1000BASE-T	R/W	1 = Force Link State machine into a link pass state. 0 = Normal operation	0
11:8	Reserved	R/W	Write as 00h, ignore when read.	0h
7	Manual Swap MDI State	R/W	1 = Manually swap MDI state 0 = Normal operation	0
6:0	Reserved	R/W	Write as 00h, ignore when read.	00h

CRC Error Counter Selector

Setting this bit enables the "1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter Register (Address 14h)" on page 97 to start counting CRC errors and store the counts in register 14h.

Force Link

Setting bit 12 = 1 forces the Link State Machine into the link pass state.

Manual Swap MDI State

Setting bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Test register 1 manually swaps the MDI transmit and receive pairs during forced 100BASE-TX and 10BASE-T operation. When this bit is set, the B50612D transceiver transmits on pairs TRD[1]± and receives on TRD[0]± when operating in 100BASE-TX and 10BASE-T modes. If this bit is cleared, the B50612D transmits on pairs TRD[0]± and receives on TRD[1]± when operating in 100BASE-TX and 10BASE-T modes. This bit is ignored when the auto-negotiation is enabled.

Expansion Registers

Expansion Register 00h: Receive/Transmit Packet Counter

Expansion register 00h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 98 bits 11:0 = F00h, and read/write access is through register 15h.

Table 73: Expansion Register 00h: Receive/Transmit Packet Counter

Bit	Name	R/W	Description	Default
15:0	Packet Counter	R/W CR	Returns the transmitted and received packet count.	0000h

Packet Counter

The mode of this counter is set by bit 11 of "1000BASE-T/100BASE-TX/10BASE-T Miscellaneous Control Register (Address 18h, Shadow Value 111)" on page 106. Either receive or transmit packets are counted. This counter is cleared on read and freezes at FFFFh.

Expansion Register 04h: Multicolor LED Selector

Expansion register 04h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 98 bits 11:0 = F04h, and read/write access is through register 15h.

Table 74: Expansion Register 04h: Multicolor LED Selector

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as 00h, ignore on read.	00h
9	Flash Now	R/W SC	1 = Initiate a multicolor LED flash. This works only when the multicolor selector is set to 0111.	0
8	In Phase	R/W	1 = $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in phase. 0 = $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in opposite phase. ***Note:*** This is only valid when Multicolor LED Selector bits are set to 0000, 0010, 0011, 0110, 0111, 1000, 1001, 1010.	0

Table 74: Expansion Register 04h: Multicolor LED Selector (Cont.)

Bit	Name	R/W	Description	Default
7:4	MULTICOLOR[2] LED Selector	R/W	Selects the Multicolor mode for MULTICOLOR[2] LED 0000: Encoded link/activity LED 0001: Encoded speed LED 0010: Activity flash LED 0011: Full-duplex LED 0100: Forced off 0101: Forced on 0110: Alternating LED (toggling between two of the states at 50% duty cycle with a 320 ms period) 0111: Flashing LED (toggling between 2 of the states with an 80 ms period) 1000: Link LED 1001: Activity LED 1010: Programmable blink LED	0h
3:0	MULTICOLOR[1] LED Selector	R/W	Selects the Multicolor mode for MULTICOLOR[1] LED 0000: Encoded link/activity LED 0001: Encoded speed LED 0010: Activity flash LED 0011: Full-duplex LED 0100: Forced off 0101: Forced on 0110: Alternating LED (toggling between 2 of the states at 50% duty cycle with a 320 ms period) 0111: Flashing LED (toggling between 2 of the states with an 80 ms period) 1000: Link LED 1001: Activity LED 1010: Programmable blink LED	0h

Flash Now

Asserting this bit causes a single flash to occur on either MULTICOLOR[2:1] LED, as long as its multicolor selector is set to 0111.

In Phase

When both LEDs are selected to the same mode, the MULTICOLOR[2:1] output pins toggle at the same time. This bit determines whether the pins are identical to each other or are inverses of each other. When the two LED pins are attached to a special multicolored LED, the resulting LED colors alternate either between off/amber (in phase) or red/green (out of phase).

MULTICOLOR[2] LED Selector

The bits [7:4] select the multicolor LED mode for MULTICOLOR[2]. The user must determine what functions should appear on the two LED pins.

Example: For a different color toggling operation than the operation previously mentioned (such as red/amber), the user can put one of the selectors to the preferred toggle mode and other selector to a forced one.

MULTICOLOR[1] LED Selector

Bits [3:0] select the multicolor LED mode for MULTICOLOR[1].

Expansion Register 05h: Multicolor LED Flash Rate Controls

Expansion register 05h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 98 bits 11:0 = F05h, and read/write access is through register 15h.

Table 75: Expansion Register 05h: Multicolor LED Flash Rate Controls

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as 0h, ignore on read.	0h
11:6	Alternating Rate	R/W	Determines the width and gap for multicolor LED selector 0110 (alternating LED mode). 00h = 21 ms width, 21 ms gap 01h = 42 ms width, 42 ms gap 02h = 63 ms width, 63 ms gap ... 07h = 168 ms width, 168 ms gap ... 3Fh = 1.344s	07h
5:0	Flash Rate	R/W	Determines the width and minimum gap of every flash pulse for multicolor LED selector 0000 (encoded link/Activity mode), 0010 (Activity Flash mode) and 0111 (Flashing LED mode). 00h = 21 ms width, 21 ms gap 01h = 42 ms width, 42 ms gap 02h = 63 ms width, 63 ms gap ... 3Fh = 1.344s	01h

Alternating Rate

Setting Bits [11:6] changes the width and gap of the alternating LED modes. These bits are only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0110. The duty cycle of the LEDs is exactly 50%.

Flash Rate

Setting Bits [5:0] determines the width and minimum gap of the flashing pulse. These bits are only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111. The duty cycle of the flash rate is not exactly 50%.

Expansion Register 06h: Multicolor LED Programmable Blink Controls

Expansion register 06h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 98 bits 11:0 = F06h, and read/write access is through register 15h.

Table 76: Expansion Register 06h: Multicolor LED Programmable Blink Controls

Bit	*Name*	*R/W*	*Description*	*Default*
15:6	Reserved	R/W	Write as 000h, ignore on read.	000h
5	Blink Update Now	R/W	1 = Change to the new blink rate now. 0 = Wait 1s before changing the blink rate. Controls when a change in the blink rate is actually displayed on the Programmable Blink LED.	0
4:0	Blink Rate	R/W	Programs the number of blinks per second of the Programmable Blink LED 00000 = No blink 00001 = 1 blink per second 00010 = 2 blinks per second 00011 = 3 blinks per second ... 11111 = 31 blinks per second	00000

Blink Update Now

Setting bit 5 updates the blink rate immediately. Clearing this bit causes the blink rate to be updated after the 1s interval timer expires. This bit is only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111.

Blink Rate

Setting bits [4:0] determines the blink rate of the Programmable Blink LED. These bits are only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111.

Expansion Register 08h: 10BT Controls

Expansion register 08h is enabled by writing to "1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h)" on page 98 bits 11:0 = F08h, and read/write access is through register 15h.

Table 77: Expansion Register 08h: 10BT Controls

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as 000h, ignore on read.	000h
9	Auto Early DAC Wake	R/W	1 = Turn on automatic early DAC wake power savings mode. 0 = Turn off automatic early DAC wake power savings mode.	1
8:0	Reserved	R/W	Write as 001h, ignore on read.	001h

Auto Early DAC Wake

Setting bit 9 = 1 turns on automatic early DAC wake power savings mode. Setting bit 9 = 0 turns off automatic early DAC wake power savings mode

Top-Level Expansion Registers

Top-Level Expansion Register 34h: Spare Register 0

Top-Level Expansion register 34h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h) bits 11:0 = D34h. Read/write access is through register 15h.

Table 78: Top-Level Expansion Register 34h: Spare Register 0

Bit	Registers name	R/W	Description	Default
15:8	Reserved	R/W	Reserved	00h
7	ADC monitor selector	R/W	1 = Select RX side 0 = Select TX side Active only when bit 6 is set to 1	0
6	ADC monitor mode enable	R/W	1 = Enable alternative ADC monitor mode	0
5:2	Reserved	R/W	Reserved	0h
1	clk125 output select	R/W	Mux clk125 output to LED4 pad	0
0	Reserved	R/W	Reserved	1

Top-Level Expansion Register 40h: 2K Buffer Register 1

Top-Level Expansion register 40h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h) bits 11:0 = D40h. Read/write access is through register 15h.

Table 79: Top-Level Expansion Register 40h: 2K Buffer Register 1

Bit	Registers name	R/W	Description	Default
15:11	Reserved	R/W	Reserved	00h
10:8	Wait_IFG_Length	R/W	Configurable number of IDLE symbols required before asserting local LPI request. • 1000BASE-T: 1 µs to 1s • 100BASE-TX: 1 µs to 5s	0h
7:3	Variable_IFG_Length	R/W	Programmable IPG of 9–128 bytes used to flush the buffer in variable latency mode. IPG is Variable_IFG_Length x 4. Minimum IPG from IEEE specification is 96 bits (12 bytes). If the MAC-transmitted IPG is smaller than the programmed value, the PHY preserves the original IPG value.	00h
2	Variable_Latency_En	R/W	When set to 1, transmit the packet from the buffer using the configured IPG, variable_IFG_length.	0
1	Reserved	R/W	Reserved	0
0	AutogrEEEn Enable	R/W	• When set to 0, disable AutogrEEEn. • When set to 1, enable AutogrEEEn.	1

Wait_IFG_Length

Wait_IFG_Length[2:0] settings are listed in Table 80.

Table 80: Wait_IFG_Length Settings

Wait_IFG_Length[2:0]	Time Before Local LPI Request (in 1000BASE-T and 100BASE-TX)
000	1.024 µs
001	4.096 µs
010	65.5 µs
011	524 µs
100	16.8 ms
101	268 ms
110	1.7s
111	4.3s

Top-Level Expansion Register 41h: 2K Buffer Register 2

Top-Level Expansion register 41h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access Register (Address 17h) bits 11:0 = D41h. Read/write access is through register 15h.

Table 81: Top-Level Expansion Register 41h: 2K Buffer Register 2

Bit	Registers name	R/W	Description	Default
15:13	Reserved	R/W	Reserved	0h
12	test_2k_ram	R/W	–	0
11	test_mii_buffer	R/W	–	0
10	Reserved	R/W	Reserved	0
9	adfauto_disable_mode	R/W	–	0
8	ovstb	R/W	–	1
7:4	tm	R/W	–	0h
3	force_rx_bypass	R/W	–	0
2:0	Wake state timer	R/W	–	0h

Clause 45 Registers

Clause 45 registers are accessed in the Clause 22 register space according to the method in Clause 22.2.4.3.11-12 and Annex 22D.

Example: To advertise EEE mode supported for 1000BASE-T and 100BASE-TX, Clause 45 DEVAD 7.3Ch bits 2:1 must be set to 11. To perform this write, the following sequence may be used:

1. In register 0Dh, write bits 15:14 = 00 (set the function field to Address) and set bits 4:0 to 00111 to set DEVAD to 7. (Write 007h to register 0Dh).
2. In register 0Eh, write the desired address value. In this example, write 003Ch to register 0Eh.
3. In register 0Dh, write 01 to the function field (bits 15:14) for Data, do not post increment. (Set DEVAD to 7: Write 4007h to register 0Dh.)
4. In register 0Eh, write the content of the register. (Write 0006h to register 0Eh to set bits 2:1 = 11.)

Example: To read the EEE Resolution Status register (Clause 45 DEVAD 7 register 803Eh), the following register sequence may be followed:

1. Write 00 to register 0Dh bits 15:14 to set the function field to Address, and set bits 4:0 to 00111 to set DEVAD to 7.
2. Write 803Eh to register 0Eh to select the EEE Resolution Status register.
3. Write C007h to register 0Dh to set the function to Data, no post increment, and to set the Device Address to 7.
4. Read register 0Eh to read the content of the selected Clause 45 register (the EEE Resolution Status register in this case).

Clause 45 Device 7 Register Address 3Ch: EEE Advertisement Register

Table 82: EEE Advertisement Register

Bit	Name	R/W	Description	Default
15:3	Reserved	R/W	Write as 0, ignore on read.	0000h
2	1000BASE-T EEE	R/W	1 = Advertise PHY has EEE capability for 1000BASE-T. 0 = Do not advertise PHY has EEE capability for 1000BASE-T.	1
1	100BASE-TX EEE	R/W	1 = Advertise PHY has EEE capability for 100BASE-TX. 0 = Do not advertise PHY has EEE capability for 100BASE-TX.	1
0	Reserved	R/W	Write as 0, ignore on read.	0

1000BASE-T EEE

This bit, when set, turns on advertisement for 1000BASE-T EEE mode. EEE mode is turned off by default. Register 09h bits 9:8 must be set to advertise 1000BASE-T mode and auto-negotiation must be restarted for EEE mode to take effect.

100BASE-TX EEE

This bit, when set, turns on advertisement for 100BASE-TX EEE mode. EEE mode is turned off by default. Register 04h bits 8:7 must be set to advertise 100BASE-TX mode and auto-negotiation must be restarted for EEE mode to take effect.

Clause 45 Device 7 Register Address 803Dh: EEE Control Register

Table 83: EEE Control Register

Bit	Name	R/W	Description	Default
15	LPI_Feature_En	R/W	When bit 15 is set to 1, it enables the EEE feature. If bit 15 is cleared to 0, the EEE feature is disabled.	1
14:0	Reserved	R/W	Write as 0, ignore on read.	0000h

Clause 45 Device 7 Register Address 803Eh: EEE Resolution Status Register

Table 84: EEE Resolution Status Register

Bit	Name	R/W	Description	Default
15:3	Reserved	RO	Write as 0, ignore on read.	000
2	EEE_1000T_Resolution	RO	If bit returns 1 and auto-negotiation is enabled, both local device and link partner advertise EEE capability in 1000T mode. If bit returns 1 and auto-negotiation is disabled, local device is EEE capable in 1000T mode. If bit returns 0 and auto-negotiation is enabled, no EEE capability in 1000T mode is advertised on local device or link partner. If bit returns 0 and auto-negotiation is disabled, no EEE capability in 1000T mode is reported on local device.	0
1	EEE_100TX_Resolution	RO	If bit returns 1 and auto-negotiation is enabled, both local device and link partner advertise EEE capability in 100BASE-TX mode. If bit returns 1 and auto-negotiation is disabled, local device is EEE capable in 100BASE-TX mode. If bit returns 0 and auto-negotiation is enabled, no EEE capability in 100BASE-TX mode is advertised on local device or link partner. If bit returns 0 and auto-negotiation is disabled, no EEE capability in 100BASE-TX mode is reported on local device.	0
0	Reserved	RO	Write as 0, ignore on read.	0

Clause 45 Device 7 Register Address 803Fh: LPI Mode Counter Register

Table 85: EEE Resolution Status Register

Bit	Name	R/W	Description	Default
15:0	LPI_Mode_Counter	R/W	Counts number of lpi mode occurrences. Counter is non rollover. Maximum value of the counter is 0xFFFF. Counter is cleared on each read.	0000h

Section 5: Timing and AC Characteristics

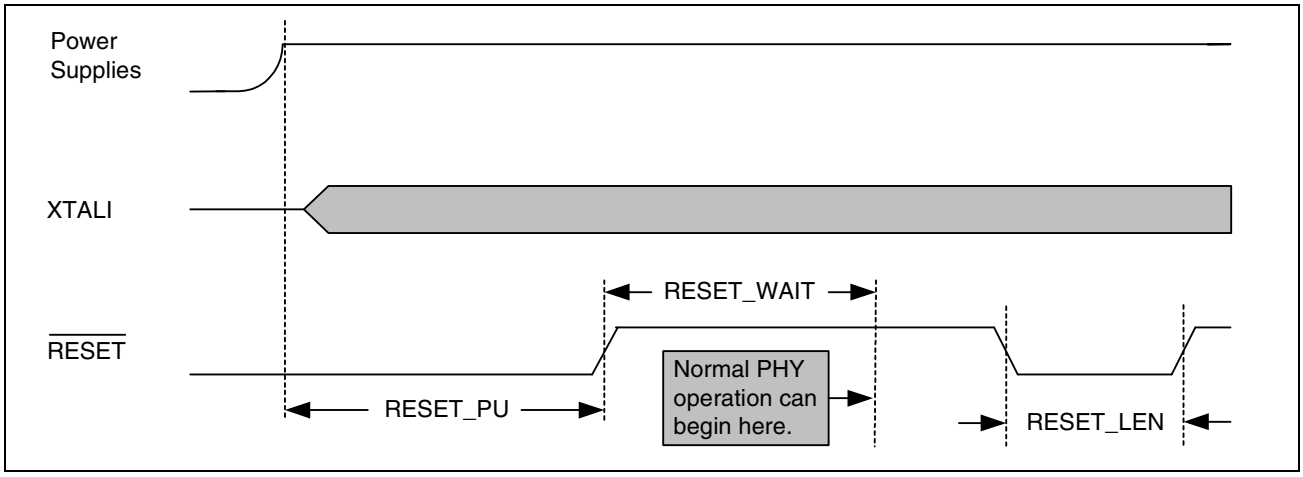
Table 86: Reset Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Power up to $\overline{\text{RESET}}$ deassertion	RESET_PU	10	–	–	ms
$\overline{\text{RESET}}$ deassertion to normal PHY operation	RESET_WAIT	20	–	–	µs
$\overline{\text{RESET}}$ pulse length	RESET_LEN	2	–	–	µs
$\overline{\text{RESET}}$ rise/fall time	–	–	–	25	ns

Note:

- When $\overline{\text{RESET}}$ is low the following also needs to be true: Valid clock signal at the XTALI input.
- All external power supplies need to be stable.
- Internal regulator output REGOUT need approximately 1 ms to stabilize after the voltage to the regulator input pin REGSUPPLY is stable.
- MII register read/write access and normal PHY operation can start at the end of the RESET_WAIT time.
- RESET_PU must be performed when the device is first powered up. Software reset or RESET_LEN do not need to be performed after RESET_PU.
- Software reset or RESET_LEN should not be performed until after RESET_PU and RESET_WAIT have been completed. After issuing a software reset or a RESET_LEN, normal PHY operation can begin after waiting RESET_WAIT time of 20 µs.

Figure 11: Reset Timing



REFCLK Input Timing

Table 87: REFCLK Input Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Frequency	C_{freq}	–	25	–	MHz
Accuracy	–	–50	–	+50	ppm
Duty Cycle Distortion[a]	–	40	–	60	%
Rise/Fall time[b]	T_r/T_f	–	–	4	ns
RMS Phase Jitter[c]	–	–	–	3	ps-rms

Note: Do not use PLL-based oscillators or zero-delay buffers as a source for REFCLK because this introduces excessive jitter that may result in unacceptable bit error rate performance.

a. Measured at 50% point.
b. Measured at the 20% to 80% points.
c. Fj = 1 kHz to 5 MHz offset frequency.

Figure 12: REFCLK Input Timing

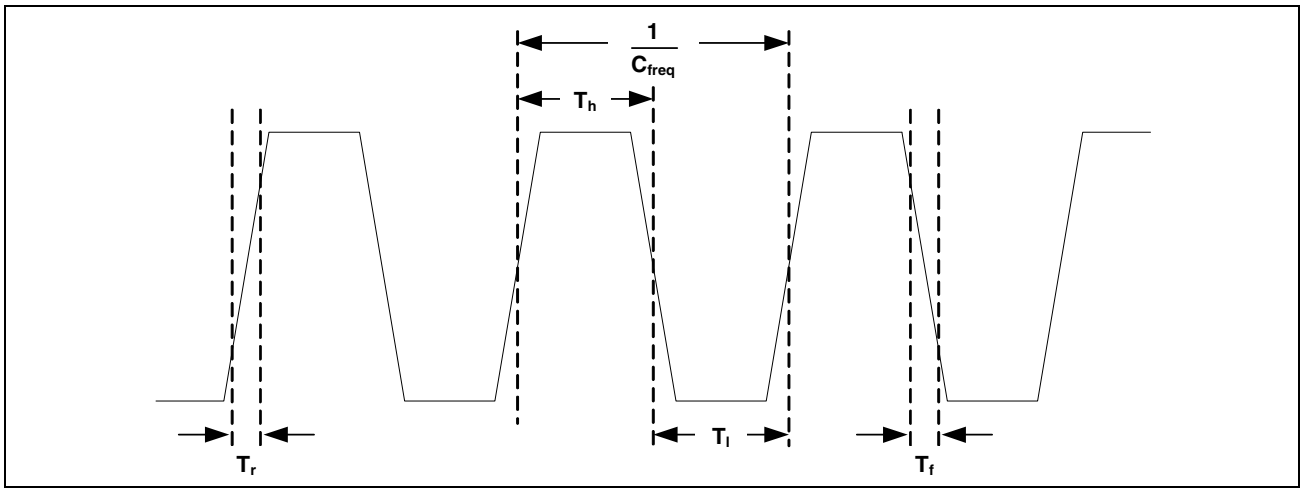


Table 88: Management Interface Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
MDC cycle time	MDC_CYCLE	80	–	–	ns
MDC high/low	–	30	–	–	ns
MDIO input setup time to MDC rising	MDIO_SETUP	10	–	–	ns
MDIO input hold time from MDC rising	MDIO_HOLD	10	–	–	ns
MDIO output delay from MDC rising	MDIO_DELAY	0	–	50	ns

Figure 13: Management Interface Timing

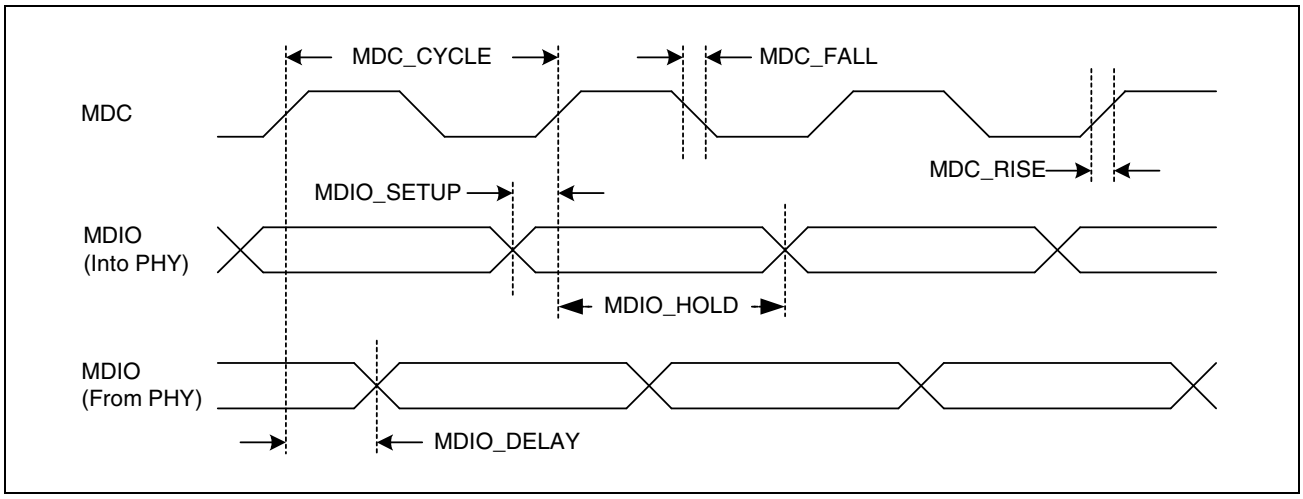


Table 89: RGMII Input Timing (Normal Mode): GTXCLK and TXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTXCLK clock period	–	–	8	–	ns
GTXCLK pulse width	–	3.6	–	–	ns
Input setup time	T_SETUP	1.0	–	–	ns
Input hold time	T_HOLD	1.0	–	–	ns

Figure 14: RGMII Input Timing (Normal Mode): GTXCLK and TXD[3:0]

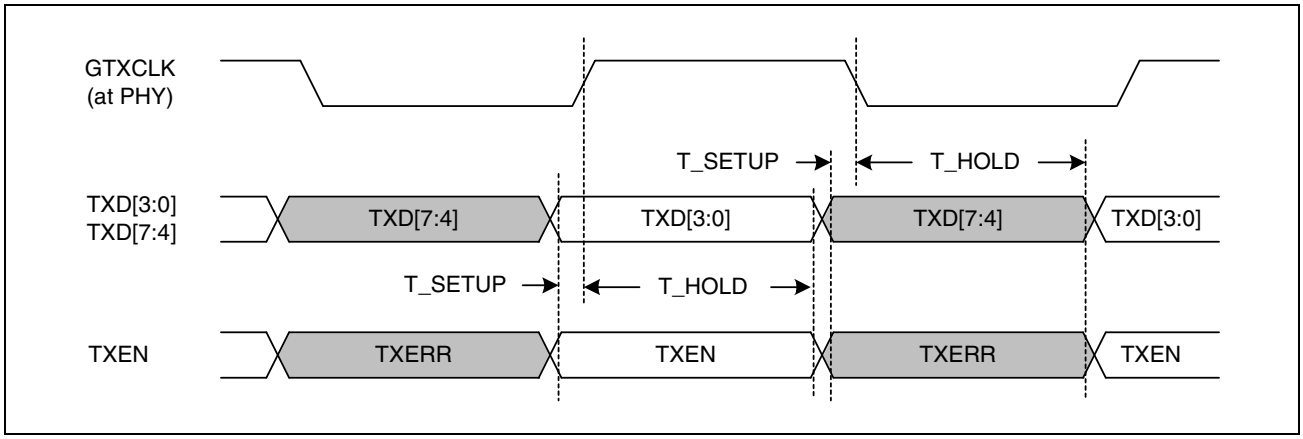


Table 90: RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTXCLK clock period	–	–	8	–	ns
GTXCLK pulse width	–	3.6	–	–	ns

Table 90: RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0] (Cont.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input setup time	T_SETUP_{DLY}	–0.9	–	–	ns
Input hold time	T_HOLD_{DLY}	2.9	–	–	ns

Figure 15: RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0]

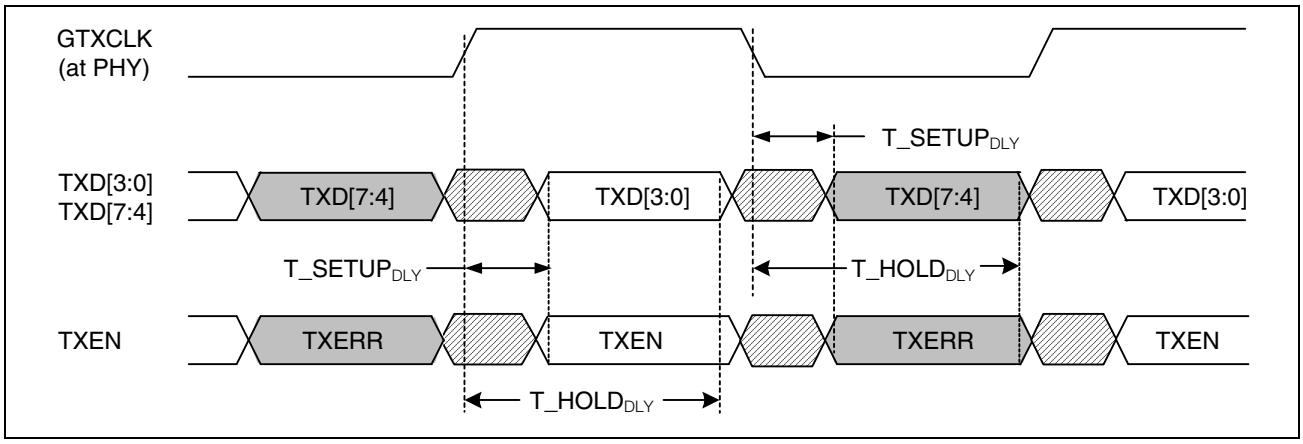


Table 91: RGMII Output Timing (Normal Mode): RXC and RXD[3:0]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
RXC clock period	–	–	8.0	–	ns
RXC clock pulse width	–	3.6	–	–	ns
Data valid to clock transition: Available setup time at the output source	T_SUAV	–0.5	–	+0.5	ns
Clock transition to data valid: Available hold time at the output source	T_HAV	3.1	–	–	ns

Figure 16: RGMII Output Timing (Normal Mode): RXC and RXD[3:0]

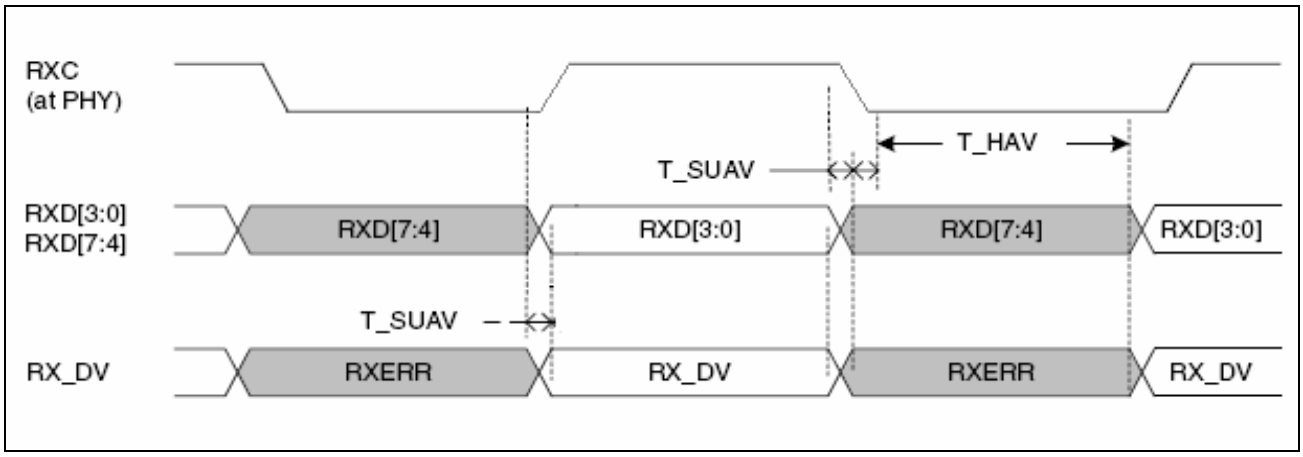
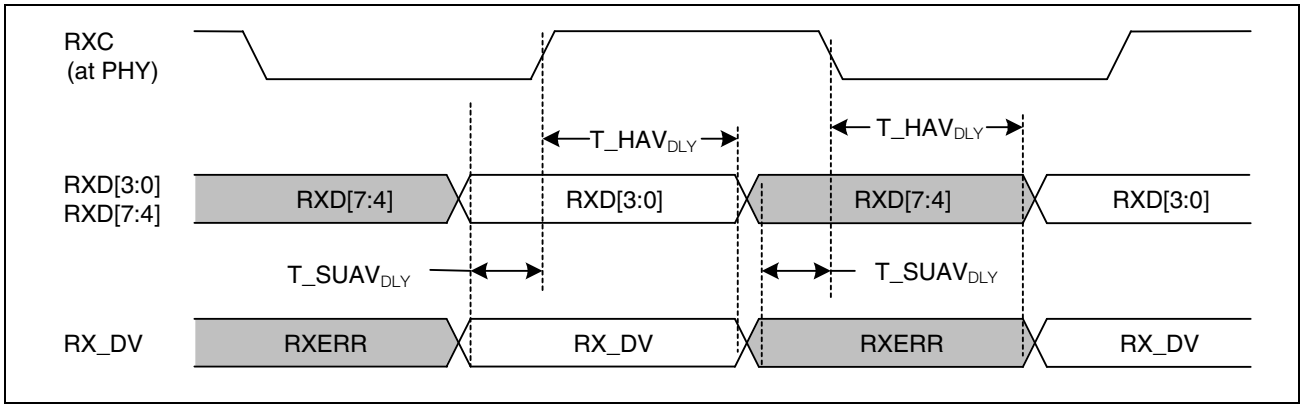


Table 92: RGMII Output Timing (Delayed Mode): RXC and RXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
RXC clock period	–	–	8.0	–	ns
RXC clock pulse width	–	3.6	–	–	ns
Data valid to clock transition: Available setup time at the output source	T_SUAV_{DLY}	1.2	2.0	–	ns
Clock transition to data valid: Available hold time at the output source	T_HAV_{DLY}	1.2	–	–	ns

Figure 17: RGMII Output Timing (Delayed Mode): RXC and RXD[3:0]



Section 6: Electrical Characteristics

Table 93: Absolute Maximum Ratings

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*
Supply voltage (OVDD, OVDD_RGMII)	–	GND – 0.3	3.8	V
Supply voltage (AVDD, PVDD, BIASVDD, XTALVDD)	–	GND – 0.3	3.8	V
Supply voltage (AVDDL, DVDD, PLLVDD)	–	GND – 0.3	1.4	V
Storage temperature	T_{STG}	-40	125	°C
ESD protection	V_{ESD}	-2000	2000	V

Note: These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 94: DC Characteristics

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Condition*
Power Supply					
Supply current 3.3V	I_{OVDD}	–	–	mA	–
Supply voltage 3.3V	V_{OVDD}	2.38	3.46	V	–
Supply voltage 3.3V	V_{OVDD_RGMII}	3.14	3.46	V	–
Supply voltage 2.5V	V_{OVDD_RGMII}	2.38	2.62	V	–
Supply voltage 1.8V	V_{OVDD_RGMII}	1.71	1.89	V	–
Supply current 3.3V	$I_{AVDD, BIASVDD, XTALVDD}$	–	–	mA	–
Supply voltage 3.3V	$V_{AVDD, BIASVDD, XTALVDD}$	3.14	3.46	V	–
Supply current 1.2V	$I_{AVDDL, DVDD, PLLVDD}$	–	–	mA	–
Supply voltage 1.2V	$V_{AVDDL, DVDD, PLLVDD}$	1.14	1.26	V	–
XTALI Pin					
Input low voltage (XTALI)	V_{IL}	-0.30	1.20	V	XTALI Pin
Input high voltage (XTALI)	V_{IH}	2.40	XTALVDD + 0.5	V	XTALI Pin
Digital Pin Operating @ 3.3V OVDD or 2.5V OVDD					
Input high voltage, digital (D) pin	V_{IH}	2.0	OVDD	V	–
Input low voltage, digital (D) pin	V_{IL}	-0.30	0.80	V	–

Table 94: DC Characteristics (Cont.)

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Condition*
Output high voltage, digital (D) pin	V_{OH}	OVDD – 0.40		V	I_{OH} = -8 mA(B1 version)/I_{OH} = -4 mA(B0 version)
Output low voltage, digital (D) pin	V_{OL}	–	0.40	V	I_{OL} = 8 mA(B1 version)/I_{OL} = 4 mA(B0 version)
LED4, digital (D) pin	V_{OH}	OVDD – 0.40		V	I_{OH} = -4 mA
LED4, digital (D) pin	V_{OL}	–	0.40	V	I_{OL} = 8 mA(B1 version)/I_{OL} = 4 mA(B0 version)
RGMII Pin Operating @ 3.3V OVDD_RGMII					
Input high voltage, RGMII (G) pin	V_{IH}	2.0	OVDD_RGMII	V	–
Input low voltage, RGMII (G) pin	V_{IL}	-0.30	0.90	V	–
Output high voltage, RGMII (G) pin	V_{OH}	2.1	–	V	I_{OH} = -1 mA
Output low voltage, RGMII (G) pin	V_{OL}	–	0.50	V	I_{OL} = 1 mA
RGMII Pin Operating @ 2.5V OVDD_RGMII					
Input high voltage, RGMII (G) pin	V_{IH}	1.70	OVDD_RGMII	V	–
Input low voltage, RGMII (G) pin	V_{IL}	-0.30	0.70	V	–
Output high voltage, RGMII (G) pin	V_{OH}	2.0	–	V	I_{OH} = -1 mA
Output low voltage, RGMII (G) pin	V_{OL}	–	0.4	V	I_{OL} = 1 mA
RGMII Pin Operating @ 1.8V HSTL OVDD_RGMII					
Input high voltage, RGMII (G) pin	V_{IH}	0.5*OVDD_RGMII+0.10	OVDD_RGMII	V	HSTL
Input low voltage, RGMII (G) pin	V_{IL}	-0.30	0.5*OVDD_RGMII-0.10	V	HSTL
Output high voltage, RGMII (G) pin	V_{OH}	OVDD_RGMII-0.40	–	V	HSTL
Output low voltage, RGMII (G) pin	V_{OL}	–	0.4	V	HSTL
$\overline{\text{RESET}}$, MDIO, MDC Pins					
Input high voltage ($\overline{\text{RESET}}$, MDIO, MDC)	V_{IH}	2.0	OVDD	V	$\overline{\text{RESET}}$, MDIO, MDC pins
Input low voltage ($\overline{\text{RESET}}$, MDIO, MDC)	V_{IL}	-0.30	0.80	V	$\overline{\text{RESET}}$, MDIO, MDC pins
Hysteresis at 3.3V OVDD	V_{HYST}	150	400	mV	$\overline{\text{RESET}}$, MDIO, MDC pins

Table 94: DC Characteristics (Cont.)

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Condition*
Hysteresis at 2.5V OVDD	V_{HYST}	90	400	mV	$\overline{\text{RESET}}$, MDIO, MDC pins

Section 7: Mechanical and Thermal

RoHS-Compliant Packaging

Broadcom offers both a standard package and an RoHS package that is compliant with RoHS and WEEE directives. Standard parts are also compliant with these directives, except for Pb (>1000 ppm). Table 95 shows the main differences between standard and RoHS-compliant parts.

RoHS-compliant parts have the letter G added to the top line of the part marking. Standard parts (non Pb-free parts) are NOT compatible with the Pb-free surface-mount process. Refer to the *Pkg Reflow Process Guidelines for Surface Mount Assemblies Application Note* (PACKAGING-AN10*X*-R) for more details.

Table 95: Main Differences Between Standard and RoHS-Compliant Packages

Part Number	*Package*	*Solder Composition/Lead Plating Composition*	*Maximum Reflow Temperature*
B50612DB1KMLG	48-pin MLP (RoHS compliant package)	100% Sn (Matte)	260°C

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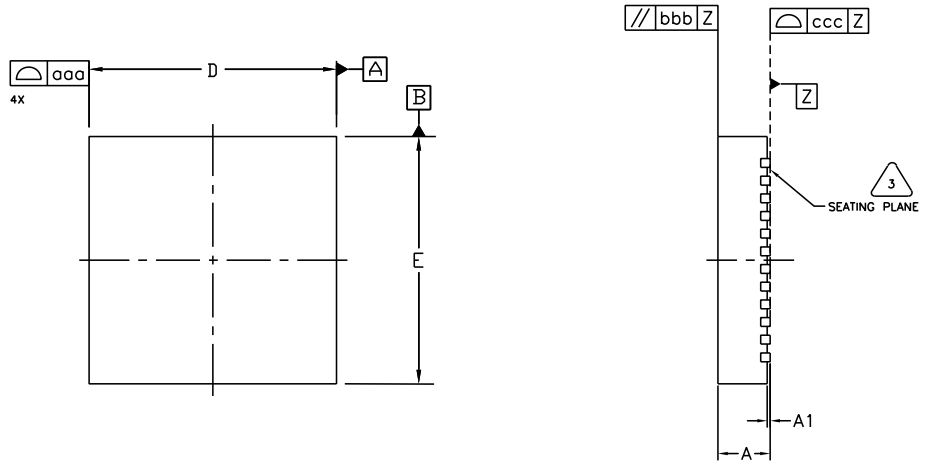
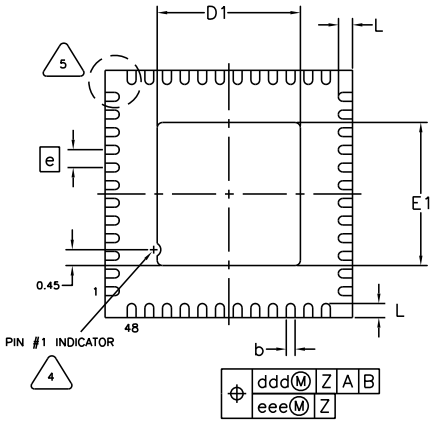
Mechanical Information

Figure 18: 48-Pin MLP Package



TOP VIEW

SIDE VIEW



BOTTOM VIEW
(48 LEADS)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.025	0.05
D	6.90	7.00	7.10
D1	3.95	4.05	4.15
E	6.90	7.00	7.10
E1	3.95	4.05	4.15
b	0.18	0.25	0.30
e		0.50 BSC	
L	0.35	0.40	0.45
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD-xxx-yyyy-000

5 EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.

4 EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY

3 APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING

2. MAX COPLANARITY IS 0.05mm AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Note: Refer to PACKAGING-AN20x-R for copper land layout and soldering guidelines.

Thermal Information

This section includes basic thermal information pertaining to the B50612D in the 48-pin MLP package.

Table 96 provides a comparison of Theta-J_A versus airflow for the 48-pin MLP package. Theta-J_C for this package is 28.2°C/W. Theta-J_B for this package is 4.4°C/W. The B50612D 48-pin MLP is designed and rated for a maximum junction temperature of 125°C.

Table 96: Theta-J_A Versus Airflow for the 48-pin MLP Package

	Air Flow (feet per minute)				
48-pin MLP Package	***0***	***100***	***200***	***400***	***600***
Theta-J_A (°C/W)	32.83	30.07	29.01	27.73	27.06
PSI-JT	3.15	3.21	3.29	3.55	3.66

Section 8: Ordering Information

Table 97: Ordering Information

Part Number	*Package*	*Ambient Temperature*
B50612DB1KMLG	48-pin MLP (RoHS compliant package)	0°C to +70°C

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Appendix A: Acronyms and Abbreviations

For a more complete list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Table 98: Acronyms and Abbreviations

Term	*Description*
ESD	Electrostatic Discharge
JTAG	Joint Test Action Group
MAC	Media Access Control
MDC	Management Data Cock
MDI	Medium Dependent Interface
MDIO	Management Data Input/Output
OP	Operation Code
PHY	Physical Layer
RGMII	Reduced Gigabit Media Independent Interface
ST	Start-of-Frame
TA	Turn Around

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