Intel Programmable Acceleration Card (PAC) with Intel Arria 10 GT FPGA Datasheet


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Contents

1. Introduction

Figure 1. Intel® Programmable Acceleration Card with Intel® Arria® 10 GT FPGA

This datasheet describes the Intel® Programmable Acceleration Card (PAC) with Intel Arria® 10 GT FPGA, featuring the Intel Arria 10 GT FPGA. This document shows electrical, mechanical, compliance, and other key specifications. This datasheet assists network operators and system integrators to properly deploy this PAC into their servers. It also documents the FPGA power envelope, connectivity speeds to memory, and network connectivity, so that accelerator function unit (AFU) developers can properly design and test their IP.

The PAC is supported by the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs. The Intel Acceleration Stack provides a common developer interface to both application and acceleration function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA factory image.

For information about using the Intel Acceleration Stack for Intel Xeon CPU with FPGAs, refer to the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GT FPGA*.

Note: Contact your Intel field sales representative for EAP documentation for the Intel PAC with Intel Arria 10 GT FPGA.

Along with acceleration libraries and development tools, the Acceleration Stack saves development time and enables code re-use across multiple Intel FPGA form-factor products, allowing the developer to focus on the unique value-addition of their solution.

Intel validates each Intel Programmable Acceleration Card with Intel Arria 10 GT FPGA to support large scale deployments requiring FPGA acceleration. This platform is targeted for market-specific acceleration in applications such as:

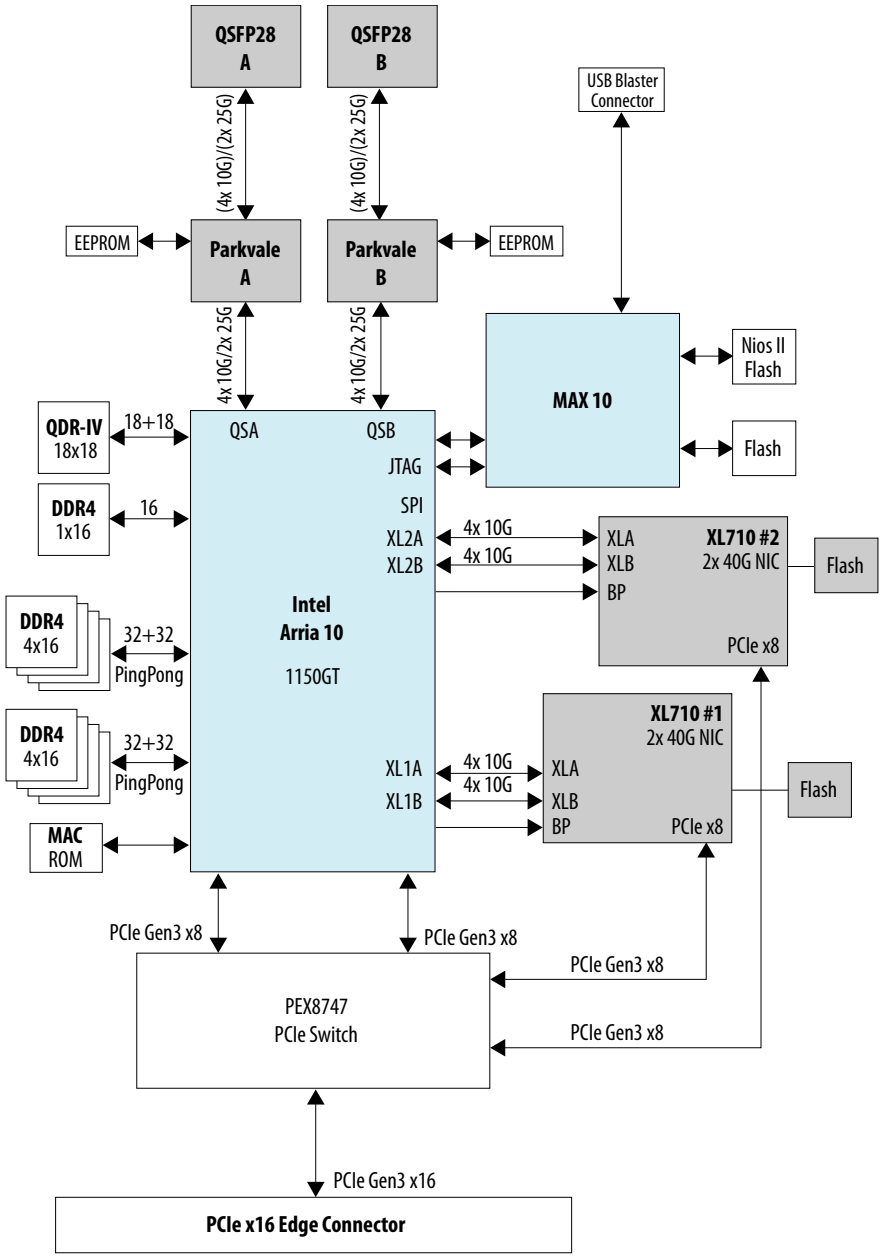
- Network Function Virtualization (NFV)
- Multi-Access Edge Computing (MEC)
- Video Transcoding
- Cyber Security
- High-Performance Computing
- Finance

2. Overview

This chapter provides an overview of the programmable acceleration card and describes the board architecture and its components.

2.1. Intel PAC with Intel Arria 10 GT FPGA Block Diagram

Figure 2. Intel PAC with Intel Arria 10 GT FPGA Functional Components



2.2. Overview of Product Features

2.2.1. Intel Arria 10 GT FPGA

The Intel Arria 10 FPGAs feature industry-leading programmable logic built on 20 nm process technology that integrates a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers and IP protocol controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Intel Arria 10 FPGAs to deliver floating point performance of up to 1.5 TFLOPS. Arria 10 FPGAs have a comprehensive set of power-saving features. Combined, these features allow developers to build a versatile set of acceleration solutions.

When developing the accelerator function for the Intel PAC, select the 10AT115S1F45E1SGJZ device.

Related Information

- Intel FPGA Devices
  Detailed information about features of the Intel Arria 10 FPGA family
- Intel Arria 10 Device Datasheet
  This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel Arria 10 devices.
- Intel Arria 10 Device Overview
  This device overview provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

2.2.2. Fortville Network Interface Controller

The Fortville network interface controller (NIC) provides a hardware compatible interface with Linux drivers for networking software stacks. In addition, the Data Plane Development Toolkit (DPDK) interfaces directly via PCIe to the Fortville NIC to provide queues for high performance networking applications. With data traffic traversing the Intel Arria 10 GT to and from the Fortville NIC, you can use the Intel Arria 10 GT to perform ingress packet policing and ingress queuing, packet manipulation and addition of user defined packet tags. Similarly, the Intel Arria 10 GT can perform egress traffic shaping, queuing, and packet manipulation.

2.2.3. On-Board Memory

- 8 GB DDR4 memory
  - 2133 Mbps
  - Two 4 GB DDR4 memory banks
  - Width: 64 bits
- 1 GB DDR4 memory
  - 2133 Mbps
  - Width: 16 bits
- One 144 megabit (Mb) QDR-IV memory
  - 933 MHz
  - 8M × 18
- One 1 Gbit flash – for use with the FPGA factory image

2.2.4. Interfaces and Dimensions

- PCI Express (PCIe) Gen3 ×16

  Note: The PAC with Intel Arria 10 GT does not support PCIe Gen4.
- JTAG Header to connect to Intel FPGA Download Cable II for optional configuration of Intel Arria 10 and Intel MAX® 10 devices.

  Note: Production versions will have this interface disabled.
- 2× Quad Small Form Factor Pluggable 28 (QSFP28) with 8× 10GbE support.
- Conforms to the 1 rack unit (1U) standard in conformance with EIA-310. One rack unit is 44.5 mm (1.75 inches) high.
- ½ Length, full height card

2.2.5. Software

- Acceleration Stack for Intel Xeon CPU with FPGAs
- Factory image stored in FPGA programming flash
- Board Management Controller firmware

Related Information

Intel FPGA Acceleration Hub
Information about the Intel Acceleration Stack.

2.2.6. Power

- 100W thermal design point (TDP)
  - As the developer or solution provider, you must ensure that the AFU does not exceed the TDP limit or the limit specified by the qualified server vendor. Functionality and reliability of the server is not supported for AFUs that exceed the specification.
  - The PAC source power must be provided from both the 12V PCIe slot and the 12V Auxiliary 2×3 power connector. The PAC does not power up if either power source is disconnected.

2.2.7. Board Management Controller (BMC)

The Board Management Controller (BMC) provides the following functions:

- Board power management
- FPGA flash configuration download
- FPGA flash and BMC firmware remote system updates
- Monitoring telemetry data (board temperature, voltage and current) and reporting to the host through Platform Level Data Model (PLDM) protocol transactions

2.2.8. Network Interface

The Intel PAC with Intel Arria 10 GT FPGA has two QSFP28 cages on the front panel which support the following Ethernet network interfaces:

- 25Gbps (4×25Gbps) on QSFP A
- 10Gbps (8×10Gbps) on QSFP A and B

The PAC supports Intel validated Short Reach (SR) optical transceivers and Direct Attached Copper (DAC) cables up to 3m in length.

Table 1. QSFP+ Support for the Intel Programmable Acceleration Card with Intel Arria 10 GT FPGA

	Model Number
Intel Ethernet QSFP+ 1-meter direct attach cable (DAC) twinaxial cables	XLDACBL1
Intel Ethernet QSFP+ 3-meter direct attach cable (DAC) twinaxial cables	XLDACBL3
Intel Ethernet QSFP+ short reach (SR) optic module	E40GQSFPSR
Intel Ethernet QSFP+ 1-meter Passive Breakout Cable	X4DACBL1
Intel Ethernet QSFP+ 3-meter Passive Breakout Cable	X4DACBL3

2.2.9. Control and Support

The following features are available on this acceleration card for configuration, control and support:

- PCIe Gen3 ×16
- Board Management Controller (BMC)
- JTAG header to be used with the Intel FPGA Download Cable II

  Note: The JTAG header is available only on ES boards. It will be disabled in production hardware.

2.2.9.1. Parkvale Retimer

All network interfaces pass through the Parkvale retimer device. This device provides tightly controlled network timing performance for both 10 Gb and 25 Gb ethernet.

2.2.9.2. PCIe Overview

The communication link between the Intel PAC with Intel Arria 10 GT FPGA and a host is through a PCIe Gen3 x16 Edge Connector. The card contains a PCIe switch with multiple ports connected to different components on the PAC such as the Intel Arria 10 GT and the Ethernet Controllers.

2.2.9.3. Board Management Controller Overview

The Board Management Controller (BMC) is responsible for controlling, monitoring and giving low-level access to board features. The BMC microcontroller interfaces with on-board sensors, the FPGA and the flash. It also controls power and resets. The microcontroller communicates over PCIe I^2C using the Platform Level Data Model (PLDM) 1.1.1 protocol.

The firmware that runs on the BMC microcontroller is field upgradeable over PCIe using the remote system update feature.

BMC Features

- Power up / down sequencing and fault detection with automatic shut-down protection
- Monitoring of the status of board components (board power and component level temperature sensors)

For more details refer to the *Board Management Controller* section.

Related Information

Board Management Controller on page 17

3. System Compatibility

This section describes the platforms and Linux distribution targeted for the acceleration card validation.

Note: This section will be updated as Intel validates more server platforms.

Platforms

Table 2. Platform Validation

Servers/Systems	Description
Intel	Neon City (NC)
Dell*	R740, R640

Intel platforms have Skylake-EP and Cannonlake-EP processors in combination with the Lewisburg chipset.

Operating System Validation

Table 3. Operating System Validation

Operating Systems (OS)	OS Family
RHEL™ 7.4	RHEL
CentOS 7.4	CentOS

Note: The above mentioned Operating Systems are Linux™ Kernel 3.10

PCIe Adapters

PCIe adapters must have the following PCIe* ID and power/thermal budget.

- VID - Vendor ID
- SVID - Sub Vendor ID
- DID - Device ID
- SDID - Sub Device ID

Table 4. PCIe ID

PCIe VID	PCIe DID	PCIe SVID	PCIe SDID
0x8086	0x09C4	0x8086	0x0000
TBD	TBD	TBD	TBD

Note: The values in the table above will be updated in future revisions.

4. Mechanical Information

PAC Dimensions

- Standard height, half length PCIe card
- Maximum component height: 14.47 mm
- PCIe x16 mechanical

5. Thermal Specifications

This acceleration card is thermally limited to dissipate no more than 45 W on the FPGA. FPGA junction temperature must not exceed 95°C. Make sure the temperature of the QSFP+ module is within the vendor specification, usually 70°C or 85°C.

- Operating Temperature: 95 °C
- Shutdown Temperature: 100 °C

Note: Refer to the Power Estimator Guide to avoid exceeding 95 °C.

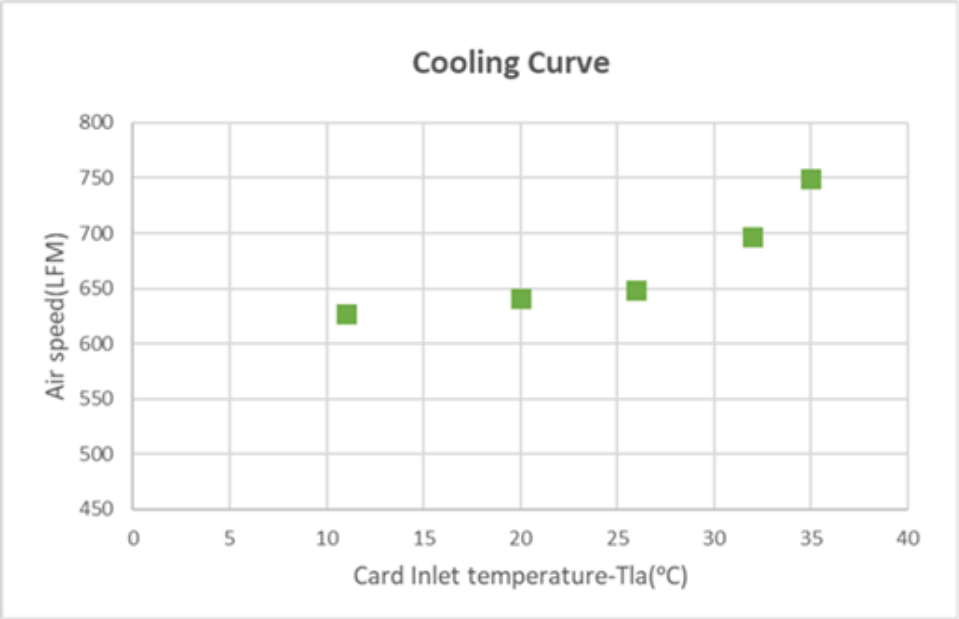
Note: AFU Developers should use the Arria 10 PowerPlay Early Power Estimator and the Quartus Prime Power Analyzer to estimate power consumption.

Figure 3. Airflow Pattern

The Intel PAC with Intel Arria 10 GT FPGA has minimum airflow requirements for corresponding card inlet air temperatures, as shown in the figure below. Each data point shows the minimum airflow (Y-axis) through the card for a corresponding card inlet temperature (X-axis).

This minimum airflow keeps the Intel Arria 10 GT junction temperature below 95°C. Providing forced air cooling is an absolute requirement to meet these minimums. These airflow requirements are based on a typical board power consumption of 66 Watts. In most server systems, you must modify the BIOS settings to enable the fans to run at 100% capacity constantly.

Figure 4. Cooling Curve



Related Information

Power Analysis and Optimization User Guide: Intel Quartus® Prime Pro Edition
The Intel Quartus® Prime Pro Edition software provides a complete design environment for FPGA and SoC designs. The Power Analyzer is described in the Power Analysis and Optimization User Guide: Intel Quartus® Prime Pro Edition.

5.1. Thermal Test Performance Results

Table 5. Terms and Descriptions

Term	Description
Linear Feet per Minute (LFM)	Air velocity is calculated by dividing the volumetric flow rate by the cross-sectional area of the flow passage.
T_{LA}	The measured ambient temperature locally surrounding the FPGA. The ambient temperature should be measured just upstream of a passive heatsink or at fan inlet for an active heatsink.

Table 6. T_{LA} vs. Velocity Profile with Air Duct

T_{LA} (°C)	Velocity (LFM) (85 °C QSFP spec)	Velocity (LFM) (70 °C QSFP spec)
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD

Table 7. T_{LA} vs. Velocity Profile without Air Duct

T_{LA} (°C)	Velocity (LFM) (85 °C QSFP spec)	Velocity (LFM) (70 °C QSFP spec)
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD

6. FPGA Factory Image

The FPGA factory image contains FPGA logic to support the accelerators, including the following:

- The PCIe IP core
- The Core Cache Interface protocol (CCI-P) fabric
- DDR4 memory interface controller IP
- QDR4 memory interface controller IP
- 10 GbE physical interface and MACs with pass-through connectivity between Parkvale and Fortville
- The management engine

Specific features of the factory image are listed in the following documents:

- *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GT FPGA*

  Note: Contact your Intel field sales representative for EAP documentation for the Intel PAC with Intel Arria 10 GT FPGA.
- OPAE Intel FPGA Linux Device Driver Architecture Guide

The 1024 Mb flash memory stores the FPGA factory image. The FPGA factory image cannot be changed in the field.

The factory image can read the FPGA temperature through the Intel Acceleration Stack.

The Intel Programmable Acceleration Card with Intel Arria 10 GT FPGA does not support partial reconfiguration. The FPGA image is a flat image that must be loaded at power up. Reloading the FPGA image requires the server to be power cycled.

7. Board Management Controller

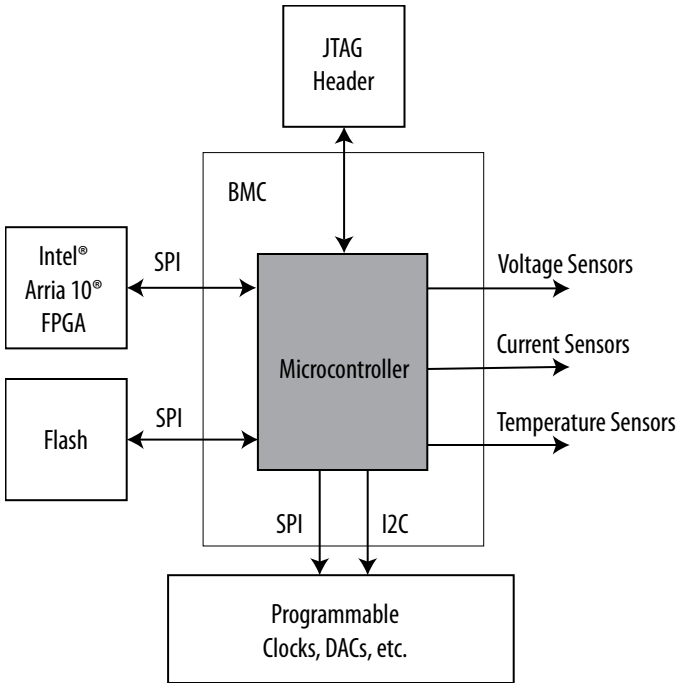
A board management controller (BMC) resides on the Intel PAC with Intel Arria 10 GT FPGA. The BMC is implemented in the Intel MAX 10 CPLD.

7.1. BMC Features

The on-board microcontroller:

- Provides low-level access to board features.
- Interfaces with sensors, FPGA, flash and QSFP.
- Controls power and resets on the board.
- Monitors temperatures, voltages and currents and provides protective action when readings are outside of critical thresholds.
- Provides Platform Level Data Model (PLDM) for PCIe I^2C communication. The I^2C slave address is 0xCE.

Figure 5. Board Management Controller for the Intel PAC with Intel Arria 10 GT FPGA



7.1.1. BMC Voltage and Thermal Handling

The BMC powers down the Intel PAC with Intel Arria 10 GT FPGA and reboots the server if the power, temperature or voltage reaches a certain threshold. This response prevents damage to the server or Intel PAC with Intel Arria 10 GT FPGA.

For threshold limits refer to the *Device Peripheral Table* section. This table shows the upper non-recoverable (UNR) value, which specifies the shutdown condition. The BMC will shut down power to the board under conditions that include the following:

- Backplane Voltage is below 10.46V
- FPGA junction temperature reaches 100°C

Note: The backplane power limits shown above are sufficient to protect the Intel PAC with Intel Arria 10 GT FPGA hardware. If your server components require more conservative limits, you can change any threshold using PLDM commands as described in *PLDM Commands for the Board Management Controller*.

To avoid unintended shutdown and loss of data:

- Use an Intel-validated server.
- Perform extensive power validation and consumption analysis on worst-case workloads.
- Use a qualified solution that is stress-tested across multiple servers and long durations.

You can identify whether the BMC has detected a board failure from the two on-board LEDs. Looking into the bracket of the Intel PAC through the venting holes on the back side of the server, you can see four steadily ON green LEDs. Behind them (further into the board), there is either a green LED or red LED that is on. The green LED blinks whenever the BMC is operating and is steadily on if the BMC is being initialized. When the BMC detects a failure condition and holds off board power, a red LED (next to the green LED) will be steadily on. Board failure conditions may occur because of an overheated FPGA or too much power draw from the board.

Related Information

PLDM Commands for the Board Management Controller on page 0

A. References

Related Information

Intel Arria 10 GX/GT Device Errata and Design Recommendations
This errata sheet provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

B. Document Revision History for Intel Programmable Acceleration Card (PAC) with Intel Arria 10 GT FPGA Datasheet

Document Version	Changes
2018.11.02	Engineering Sample (ES) Release